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1.0. Introduction :

The subject model is designed for a value line 15" color monitor. It has the following figures :

- 0.28mm dot pitch CRT, 65MHz video bandwidth ,1024x768 max resolution.
- Low radiation MPRII standard,

1.1 Electrical Characteristics

1.1.1 Power Supply	**Condition**	**Spec**	**OK**	**N.A**	**Remark**
Voltage	Universal input full range	90~264VAC /47~63Hz	√		
Input Current	90 ~ 264VAC	2.0 Arms	√		
Power consumption	On	≤ 75 W max	√		LED : Green
DPMS	Standby	≤ 5 W	√		LED : Amber Blink
	Suspend	≤ 5 W	√		LED : Amber Blink
	Off	≤ 5 W	√		LED : Amber Blink
Inrush Current	110 VAC/50Hz	40 Amp peak	√		cold-start
Leakage Current	264 VAC/50Hz	< 3.5mA	√		
Hi-Pot	1. 1500VAC, 1 sec 2. Ground test : 30A, 1sec	w/o damage < 0.1 ohm	√		(in-line test) (in-lab test)
Power cord	Length : 1800 mm	Color : Flint Gray	√		KC-003
1.1.2 Signal Interface	**Condition**	**Spec**	**OK**	**N.A**	**Remark**
Pin assignment		5V on Pin 9	√		
Video input	Level / Impedance	700mV / 75 Ohm	√		
Sync input		TTL-Positive / Negative	√		0.7 μs<H-sync width<25% of H period 2 μs<V-sync width< 400 μs
	Impedance	50 Ohm on H-sync cable	√		
Signal Cable	D-Sub	1.5M +/- 20mm	√		
	BNC			√	
	Color	Flint Gray	√		
1.1.3 Scan Range		**Spec**	**OK**	**N.A**	**Remark**
Horizontal		30 ~ 54 KHz	√		
Vertical		50~ 120 Hz	√		

1.1.4 Video Performance	Condition	Spec	OK	N.A	Remark
Dot Rate		65 MHz	√		
Max. Resolution		1024 x 768	√		
Rise time/Fall time		10 ns	√		
Video Ringing		15% max	√		
Sag		5% max	√		
Bandwidth -3db		65 MHz	√		
DDC Version		DDC1/2B	√		see table 1
EDID		Ver 2 ,Rev 1, Ver 3	√		
1.1.5 Timings	Preset mode No: 8	User mode No: 10			
Preset	**Resolution**	**Fh (KHz) / Fv (Hz)**	**OK**	**N.A**	**Remark**
VGA400	640x400	31.47KHz/70Hz	√		
VGA480	640x480	31.47KHz/59.94Hz	√		
6448A	640X480	37.5KHz/75Hz	√		
6448B	640X480	43.269KHz/85Hz		√	
SVGA4	800x600	46.88KHz/75Hz	√		
UVGA1	1024x768	48.3KHz/60Hz	√		
SVGA5	800x600	53.67KHz/85Hz	√		
Apple 16”	832x624	49.71KHz/74.533Hz		√	
UVGA2	1024x768	56.476KHz/70.069Hz		√	
UVGA7	1024x768	60.023KHz/75.029Hz		√	
Super MAC 19	1024x768	60.24KHz/75Hz		√	
UVGA8	1024x768	68.68KHz/85Hz		√	
VESA-XGA	1280x1024	63.981KHz/60.020Hz		√	
WS7	1280x1024	79.98KHz/75Hz		√	
WS8	1280x1024	91.15KHz/85Hz		√	
VESA1600	1600x1200	93.75KHz/75Hz		√	

1.2 Environment & Reliability

	Condition	Spec	OK	N.A	Remark
Operation Temp./Humidity		+10 ~ +40℃/ 20~90% R.H.	√		Non-condensing
Non-Operation Temp. / Humidity.		-20~ +60℃/ 10~95% R.H.	√		Non-condensing
Altitude	Operating condition	0~3048m (10,000ft)	√		Without packing
	Non-operating condition	0~12,192m (40,000ft)	√		With packing
Vibration 1)Sine Wave Vibration	Package, Non-Operating	5 ~ 26.6Hz /0.6g 26.6 ~ 50Hz /0.016" 50~500Hz/ 2.0g (104 Minutes/Axis for x, y, z)	√		
2)Random Vibration	Package, Non-Operating	5 ~ 100Hz, 0 dB/Oct. $0.015g^2$/Hz 100~200Hz, -6 dB/Oct., -----, 200Hz, ------ , $0.0038g^2$/Hz	√		
	Non-package, Non-Operating	20Hz~2000/ $0.0185g^2$/Hz	√		
Drop (With packing)	Package, Non-Operating	13.7kg - 76cm Height 1 corner, 3 edges, 6 faces.	√		
Electrostatic Discharge	IEC801-2 standard	Contact:8KV, Air:15KV	√		0.5~8KV tip table no blanking
Acoustical Noise		≤ 40 dB/A	√		
Power Line Transient	IEC801-4,IEC1000-4-4	Coupling clamp 0 ~ 4KV	√		
	IEC1000-4-5 (Surge)	Common:2KV, Differential:1KV	√		
	IEC1000-4-12 (100KHz ringwave)	Common:3KV, Differential:1KV		√	
MTBF Demonstration	90% confidence level	≥ 60,000 Hrs	√		Excluding the CRT
MTBF Prediction	MIL-217F	≥ 40,000 Hrs	√		Excluding the CRT
CRT Life	78% degradation	> 10000 Hrs	√		

1.3 CRT Characteristics

		Spec	OK	N.A	Remark
CRT Vender		PHILIPS	√		
Technology		FST	√		
Coating		Anti-reflection/Anti-static	√		
Dot pitch		0.28mm	√		
Phosphor		P22	√		
Light transmittance		57%	√		
Viewable size		> 13.8"	√		
Deflection angle		90 deg	√		
Blemishes and scratches		1 trio missing, as approval sheet	√		see table 2

1.4 Front of Screen

1.4.1 Geometry			**OK**	**N.A**	**Remark**
Magnetic Environment	Northern Hemisphere	H = 0 ± 0.05 V = +0.45 ± 0.05	√		
	Southern Hemisphere	H = 0 ± 0.05 V = -0.45 ± 0.05	√		
	Equatorial	H = 0 ± 0.05 V = 0 ± 0.05	√		
Size	Hor.	270 ± 4 mm	√		
	Ver.	202 ± 4 mm	√		
Centering	Hor. & Ver.	|A-B|,|C-D|< 4 mm	√		See table 4
Geometric Distortion	Top/Bottom / Side Pincushion	≤ 2 mm	√		
	Top/Bottom / Side Barreling	≤ 2 mm	√		
	Hor./Ver. Trapezoid	≤ 2 mm	√		
	Tilt	≤ 1.5 mm	√		
	Orthogonal	≤ 2 mm	√		
	S-curve	Total distortion <1.0mm	√		Max peak distortion <1.5mm
Linearity	Hor. & Ver.	≤ 5 %	√		(Xmax-Xmin)/(Xmax+Xmin)*100
1.4.2 Sharpness Crispness			**OK**	**N.A**	**Remark**
Focus	Reverse character(white background and black characters)	“e,w,m” at cut-off and 800 x 600 resolution	√		The distance of watch is 30cm from eyes to screen
Mis-convergence		A ≤ 0.3mm ,B≤ 0.4mm	√		
Moire	Over 25Ft-L	no visible moire	√		
Swing		not permitted	√		”
Jitter	DIN 66234 T2	≤ 0.1mm	√		”

1.4.3 Light Quality	Condition	Spec	OK	N.A	Remark
White Balance	Full white center (Brit. cut-off & Cont. max.)	x = 0.281 ± 0.010 y = 0.311 ± 0.010	√		@ UVGA5 800x600 53.6KHz/85Hz
Purity W,R,G,B	X max-X min & Y max-Y min	< 0.015	√		”
Color Tracking	Brightness cut off	x, y (nominal) ± 0.015	√		”
Max Brightness with ABL	Full white pattern	28Ft-L min.(Cut-off)	√		”
Max Brightness no ABL	3” Block	40Ft-L min.(Cut-off)	√		”
Brightness Uniformity	Full white pattern	≥ 70% (center to corner)	√		”
Raster light O/P	Bright./Cont. Max.	0.5 ~ 1.5Ft-L	√		”
Contrast ratio	Max/Min	5:1	√		”
1.4.4 Image Stability			**OK**	**N.A**	**Remark**
H/V regulation		≤ 1 mm per side at cut-off	√		
Flicker		No flicker	√		
Ringing		No visible DY Hor. Video ringing	√		

1.5 User Controls

1.5.1 Basic	Function	Spec	OK	N.A	Remark
	Power Switch		√		
	Contrast		√		
	Brightness		√		
	H Size		√		
	H Position		√		
	V Size		√		
	V Position		√		
	Barrel/Pincushion		√		
	Parallelogram			√	
	Trapezoid		√		
	I-Key			√	
1.5.2 Advanced	**Function**	**Spec**	**OK**	**N.A**	**Remark**
	OSD position			√	
	Color Gain			√	
	Corner			√	
	Pin-balance			√	
	Tilt			√	
	Color Temp. C1, C2	9300K, 6500K		√	
	Manual Degauss			√	
	Recall		√		
	Languages	5 languages		√	
	Mis-Convergence adj.			√	
	Moire adj.			√	
	D-sub/BNC switch			√	

1.6 Mechanical Characteristics

1.6.1 Dimension		**Spec**	**OK**	**N.A**	**Remark**
Bezel opening		212 x 283 mm	√		
Monitor w/o Stand	L x W x H mm	384 x 361 x 331 mm	√		
Monitor w Stand	L x W x H mm	384 x 361 x 384.7 mm	√		
Carton Box (outside)	L x W x H mm	474 x 440 x 420 mm	√		
Tilt and Swivel range		Tilt : -4.5/+12.5 degree Swivel:- 45/ +45 degrees	√		
1.6.2 Weight		**Spec**	**OK**	**N.A**	**Remark**
Monitor (Net)		12.0	√		
Monitor w packaging(Gross)		13.7	√		
1.6.3 Plastic		**Spec**	**OK**	**N.A**	**Remark**
Flammability		UL 94-V0	√		
Heat deflection To	ABS PC + ABS	65 ℃ 70 ℃	√		
UV stability	ABS PC + ABS	Delta E< 5 after 300Hr Xted test Delta E< 1.5 after 300Hr Xted test	√		MPR2 Model TCO Model
Resin		MPR2 : ABS TCO : PC + ABS	√		
Texture		RE-6625	√		
Color		Light Gray	√		
1.6.4 Carton		**Spec**	**OK**	**N.A**	**Remark**
Color		Kraft	√		
Material		A B Flute	√		
Compression strength		530 KGF	√		
Burst Strength		23 KGF/cm2	√		
Stacked quantity		8 Layers	√		

1.7 Pallet & Shipment

1.7.1 Dimension

Transport Type		Pallet A	Pallet B	Pallet C
Shipping Pallet Dimension(mm)	Length	1422	X	X
	Width	880	X	X
	Height	120	X	X
Air Transport Pallet Dimension(mm)	Length			X
	Width			X
	Height			X

1.7.2 Shipping Container

Stowing Type		Quantity of products (sets) (Every container)	Quantity of Products (sets) (Every Pallet)	Quantity of pallet (sets) (Every Container)
With pallet	20'	300	Pallet A: 30	Pallet A: 10
			Pallet B: X	Pallet B:
	40'	630	Pallet A: 30	Pallet A: 21
			Pallet B: X	Pallet B: X
Without pallet	20'		X	X
			X	X
	40'		X	X
			X	X

1.7.3 Air Transport Container

Container Type	Quantity of products (sets) (Every container)	Quantity of Products (sets) (Every Pallet)	Quantity of pallet (sets) (Every Container)
Container 3048 * 2260 * 2438	120	Pallet A: 30	Pallet A: 4
		Pallet B: X	Pallet B: X

1.8 Certification

	Condition	Spec	OK	N.A	Remark
Environment	Green design	API Doc. 715-C49	√		ISO14000 Requirement
	Blue Angel	German Standard		√	
	E-2000	Switzerland		√	
	NUTEK	Swedish Standard	√		
	EPA	USA Standard	√		
	EN61000-3-2 Harmonics			√	
	TCO92/95		√		
	TCO99		√		
PC-Monitor	Microsoft Windows	PC98/99	√		
	DPMS	VESA	√		
	DDC 1/2B	Version 3.0	√		
	USB	External		√	
Safety	UL (USA)	UL 1950 3rd edition	√		
	CSA (Canada)	C22.2 No. 950-M89	√		
	DNSF	EN60950	√		
	IEC950	+A1+A2+A3+A4	√		
	EN60950	+A1+A2+A3+A4	√		
	73/23/EEC		√		
	CB (Nordics)		√		
	TUV/GS	EN60950	√		
	CCIB (China)		√		
	EIAJ/JEIDA (Japan)			√	
	NOM (Mexico)			√	
	IAA (Korea)			√	
EMC	CE Mark	89/336/EEC	√		
	FCC (USA)	Class B	√		
	EN55022	Class B	√		
	CISPR 22	Class B	√		
	VCCI (Japan)	Class B	√		
	BCIQ (Taiwan)		√		
	C-Tick (Australia)	AS3548	√		
	RRL (Korean)			√	

	Condition	Spec	OK	N.A	Remark
X- Ray Requirement	DHHS (21 CFR)	USA X- Ray Standard	√		
	DNHW			√	
	PTB	German X- Ray standard	√		
	MPRII		√		
	MPRIII		√		
Ergonomics	ZH1/618	German ergonomic	√		
	ISO 9241-3 -7 & 8		√		

1.9 Appendix Table

1.9.1.1 DDC1/2B Table

Address	Data	Description
00	00	Header
01	FF	
02	FF	
03	FF	
04	FF	
05	FF	
06	FF	
07	00	
08	06	ID Manufacturer Name =API
09	09	(EISA 3 character ID)
0A	02	ID Product Code = 5515
0B	00	(Vender Assigned code)
0C	*	ID Serial Number
0D	*	32 bits serial no.
0E	*	(use 0 if n/a)
0F	*	
10	*	Week of Manufacture (0-53),use 0 if n/a
11	*	Year of Manufacture (year - 1990)
12	01	EDID version = 1
13	01	Revision = 1
14	08	Video Input Define (see Note 1)
15	1B	Max. H. Image Size (270 mm)
16	14	Max. V. Image Size (202 mm)
17	*	(gamma*100) - 100 (see Note 3)
18	E8	DPMS (see Note 2)
19	*	Red Green Bits Rx1Rx0Ry1Ry0Gx1Gx0Gy1Gy0
1A	*	Blue White Bits Bx1Bx0By1By0Wx1Wx0Wy1Wy0
1B	*	Red x bit9-2
1C	*	Red y bit9-2
1D	*	Green x bit9-2 (see Note 3)
1E	*	Green y bits9-2
1F	*	Blue x bit9-2
20	*	Blue y bit9-2
21	*	White x bit9-2
22	*	White y bit9-2
23	A4	Established Timing I
24	48	Established Timing II
25	00	Established Timing III (see Note 4)
26	45	#1 Standard Timing Identification
27	59	800*600 85Hz

Address	Data	Description
28 29	01 01	#2
2A 2B	01 01	#3
2C 2D	01 01	#4
2E 2F	01 01	#5
30 31	01 01	#6
32 33	01 01	#7
34 35	01 01	#8
36 37 38 39 3A 3B 3C 3D 3E 3F 40 41 42 43~47	00 00 00 FE 00 4D 6F 6E 69 74 6F 72 0A 20	Detailed Timing Description # 1
48 49 4A 4B 4C 4D 4E 4F 50 51 52 53 54 55 56 57 58 59	00 00 00 FE 00 4D 6F 6E 69 74 6F 72 0A 20 20 20 20 20	Detailed Timing Description # 2

Address	Data	Description
5A	00	Detailed Timing Description # 3
5B	00	
5C	00	
5D	FE	
5E	00	
5F	4D	
60	6F	
61	6E	
62	69	
63	74	
64	6F	
65	72	
66	0A	
67	20	
68	20	
69	20	
6A	20	
6B	20	
6C	00	Detailed Timing Description #4
6D	00	
6E	00	
6F	FE	
70	00	
71	4D	
72	6F	
73	6E	
74	69	
75	74	
76	6F	
77	72	
78	0A	
79	20	
7A	20	
7B	20	
7C	20	
7D	20	
7E	00	Extension Flag
7F	*	Check sum

Note 1

Bit	Bit Description
7	Analog / Digital Signal Level
6	Signal Level Standard (6)
5	Signal Level Standard (5)
4	Setup
3	Sync Inputs Supported (3)
2	Sync Inputs Supported (2)
1	Sync Inputs Supported (1)
0	Sync Inputs Supported (0)

<table>
<tr><th>Bit</th><th colspan="2">Description</th></tr>
<tr><td>7</td><td colspan="2">Analog / Digital Input : Defines usage of the rest if the byte as "analog input" or digital input". Analog=0, Digital=1 . If input is described as analog, the following definitions apply to bits 6-0. Digital is as yet undefined in the following but provisions have been made in anticipation of a common video output standard for Flat Panel Display (FPD) use.</td></tr>
<tr><td>6:5</td><td colspan="2">Signal Level Standard (6:5) : Refer to the following bit definitions. Identified by the level of reference white volts above blank, followed by the level of the sync tips in volts below
blank.

Bit 6 / Bit 5 / Operation
0 / 0 / 0.700V/0.300V (1.000V p-p)
0 / 1 / 0.714V/0.286V (1.000V p-p)
1 / 0 / 1.000V/0.400V (1.400V p-p)
1 / 1 / Reserved; TBD</td></tr>
<tr><td>4</td><td colspan="2">Setup: If set, the display is set to expect a blank-to-black setup or pedestal per the appropriate signal level standard.</td></tr>
<tr><td>3:0</td><td colspan="2">Sync Inputs (See Bit Operation below)</td></tr>
<tr><td></td><td>3</td><td>Separate Sync</td></tr>
<tr><td></td><td>2</td><td>Composite Sync (on H Sync line)</td></tr>
<tr><td></td><td>1</td><td>Sync on Green Video</td></tr>
<tr><td></td><td>0</td><td>Serration of the V.Sync Pulse is required when composite sync or sync-on-green video is used</td></tr>
</table>

Note 2

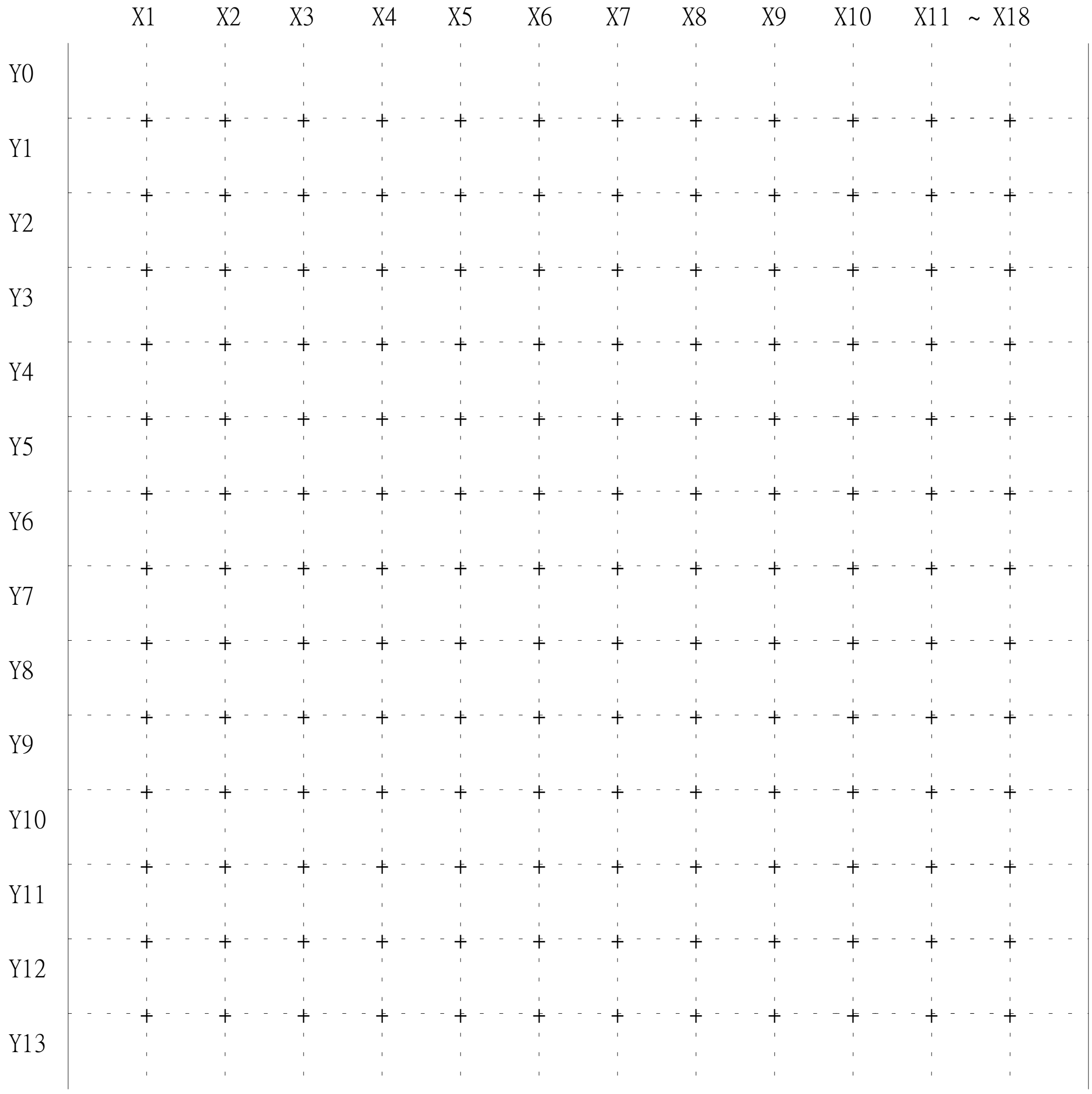
Bit 7	Stand-by
Bit 6	Suspend
Bit 5	Active off
Bit 4:3	Display Type
	0,0 - Monochrome/gray scale display 0,1 - RGB color display 1,0 - Non-RGB multicolor display (example:RGY) 1,1 - Undefined.
Bit 2:0	Reserved. Set at 00h until defined.

Note 3

CRT Vender	Chunghwa	Hitachi	Samsung	Philips	Orion
17h	BC	A6	7E	BB	E2
19h	06	0E	FB	A2	07
1Ah	4E	6E	BE	AE	4E
1Bh	A0	A0	A1	9E	A0
1Ch	57	57	55	59	57
1Dh	4F	48	4B	4E	4A
1Eh	97	99	97	99	9A
1Fh	26	26	24	27	26
20h	10	10	10	10	10
21h	47	47	47	47	47
22h	4F	4F	4F	4F	4F

Note 4 - Geometry Fig.

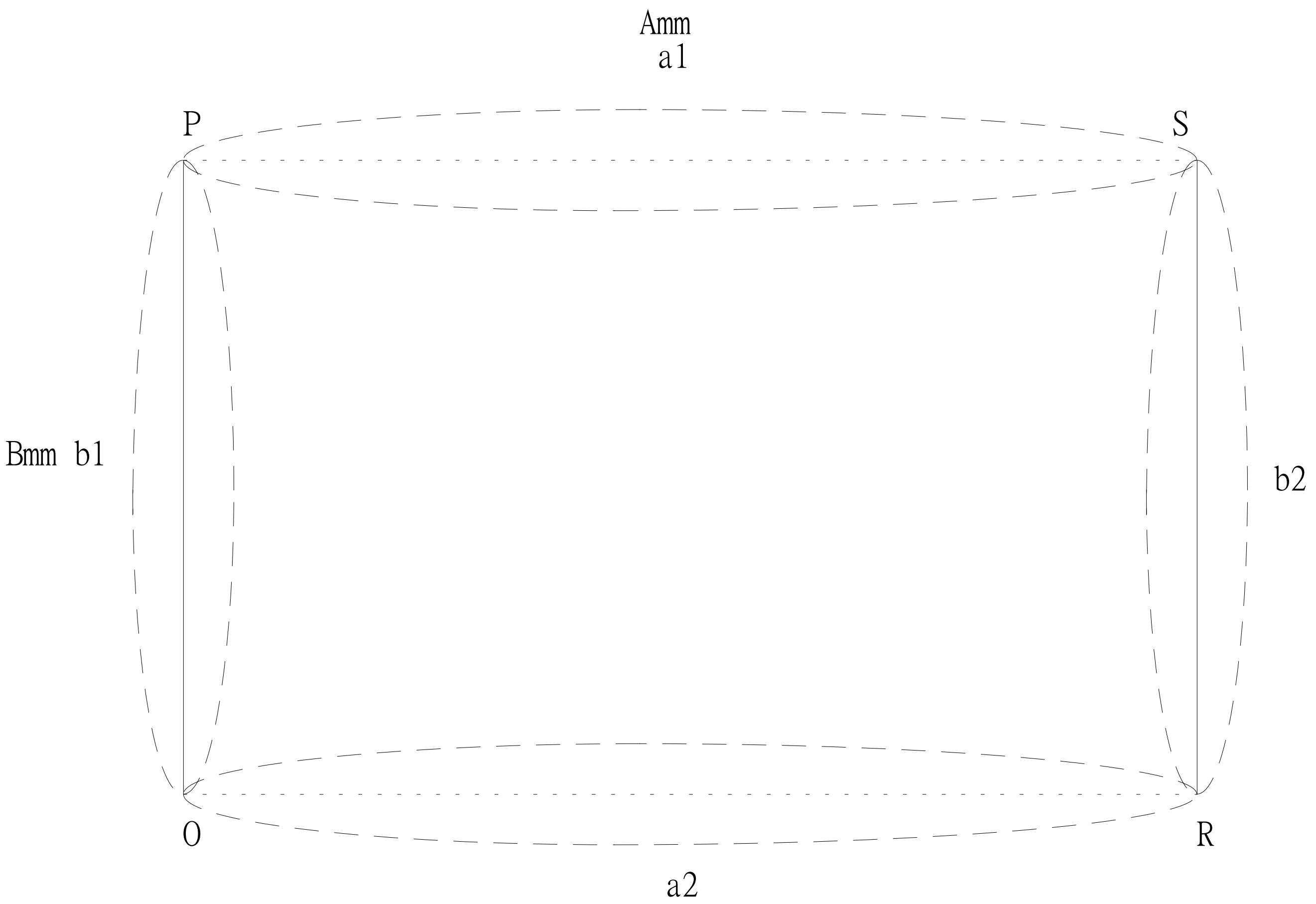
Fig.1 Linearity Measurements



$$\frac{Xmax - Xmin}{Xmax + Xmin} \text{ X } 100\% < 5\%$$

$$\frac{Ymax - Ymin}{Ymax + Ymin} \text{ X } 100\% < 5\%$$

Fig.2 General Pincushion Measurements



A, B represented as display area width and height

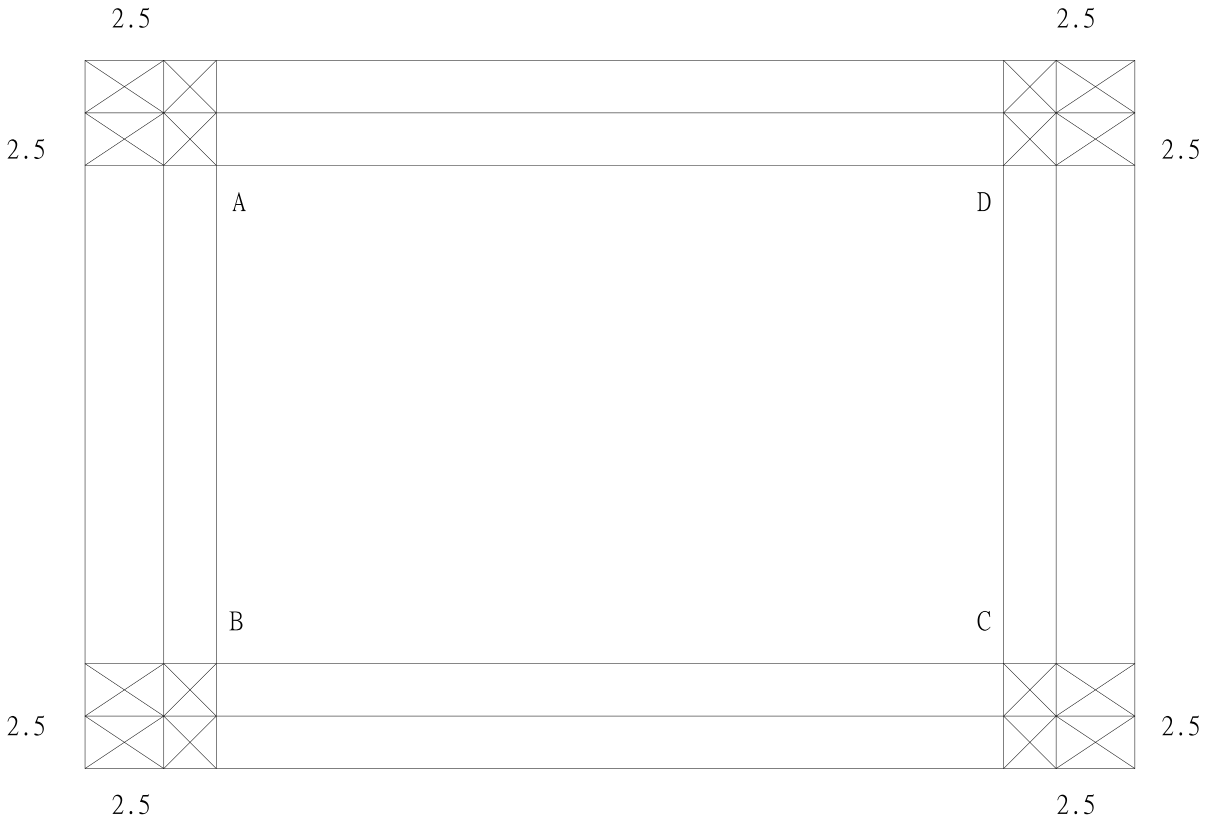
Top/Bottom Pincushion = (a1 or a2)

Side Pincushion = (b1 or b2)

Substituted A by (PS + QR)/2

B by (PQ + RS)/2

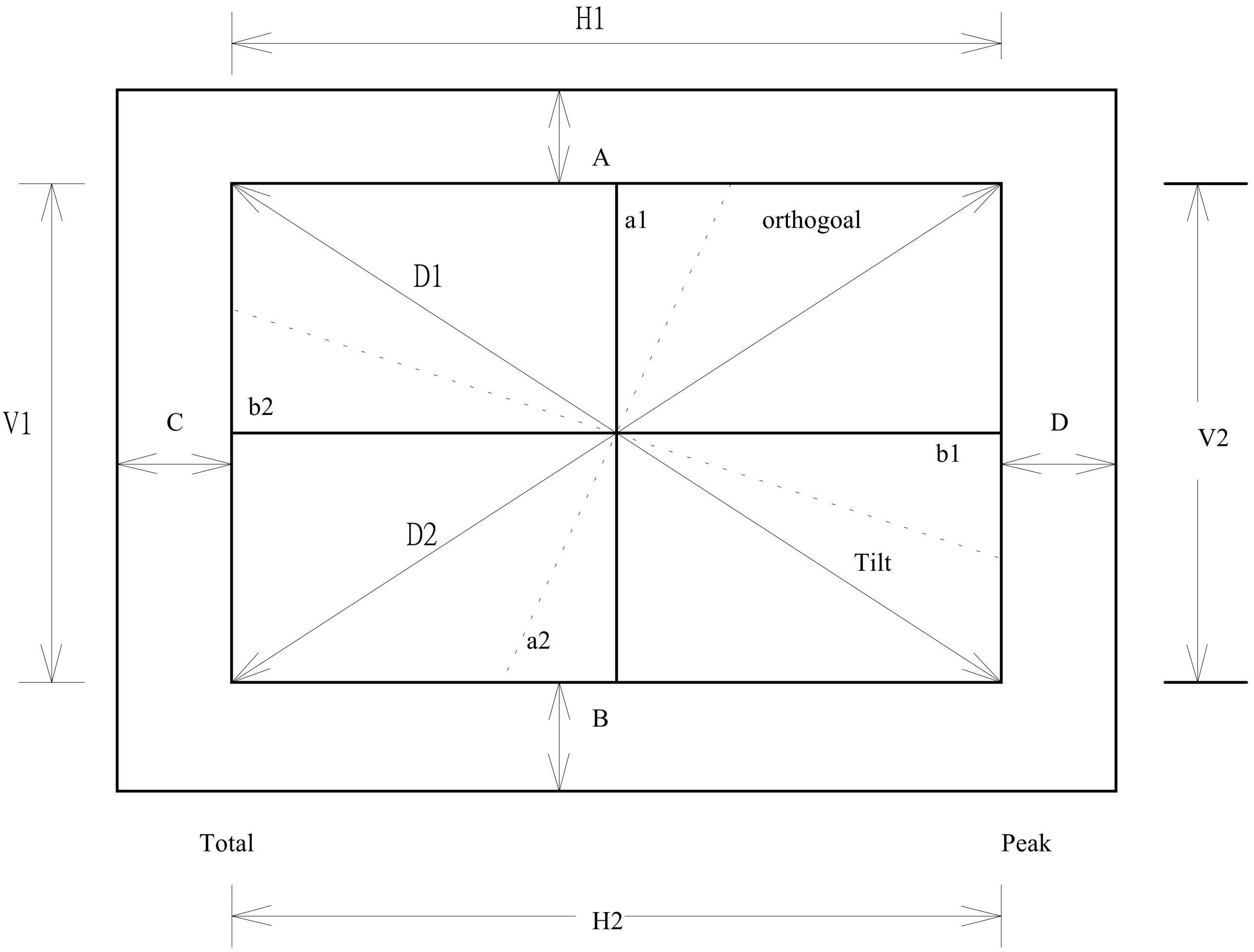
Fig.3 Trapezoid Measurements



* Each of the 4 corners of picture shall fall within the relevant area (F) illustrated up (hatched)

* ABCD is the picture outlines.

Fig.4 Picture Distortion & Phase Measurements

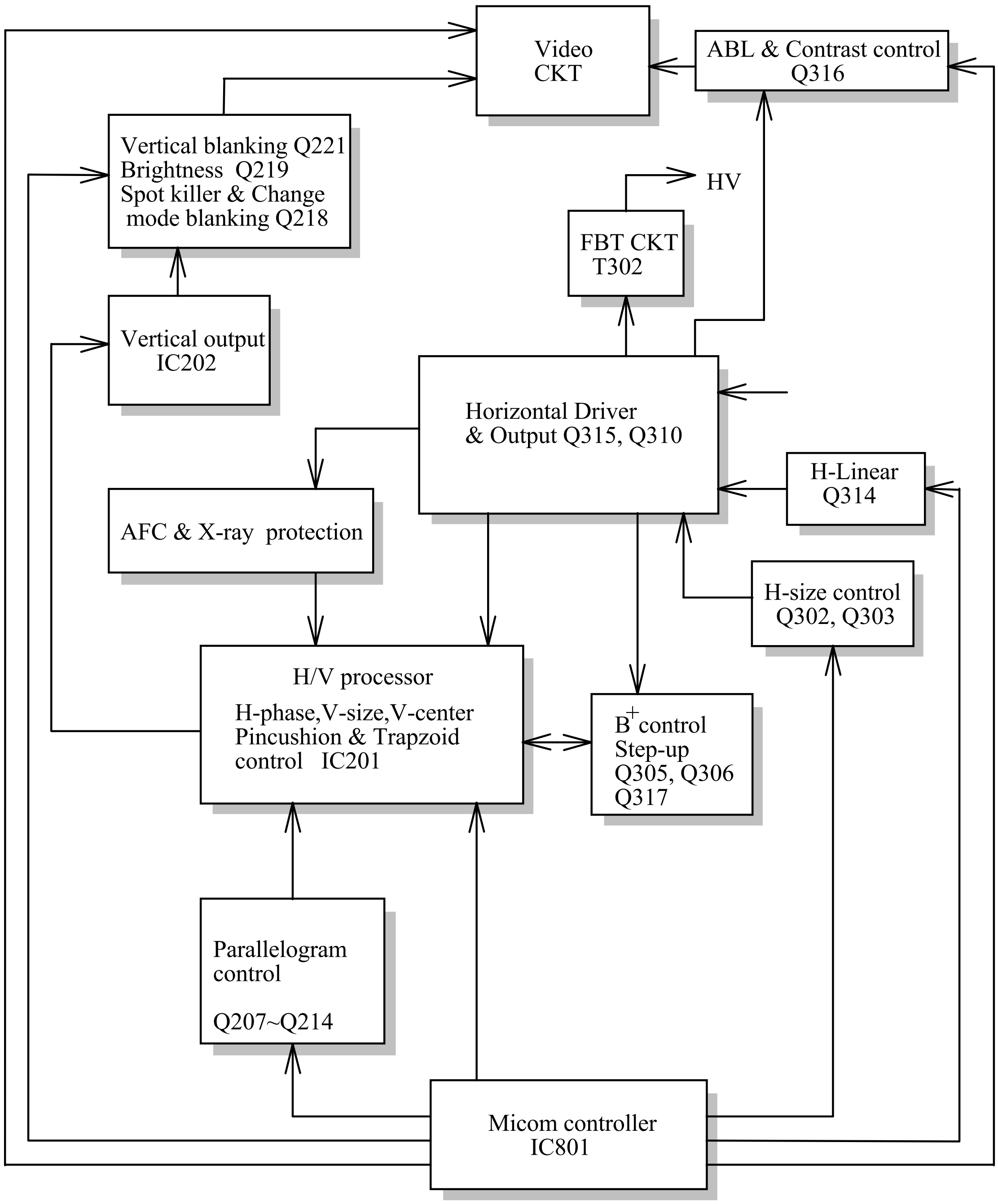


$$\frac{|H1-H2]}{0.5(H1+H2)} \leq 0.02 \qquad \frac{|V1-V2]}{0.5(V1+V2)} \leq 0.02 \qquad \frac{|D1-D2]}{0.5(D1+D2)} \leq 0.03$$

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2.1 Defection CKT

2.1.1 Block Diagram of Defection

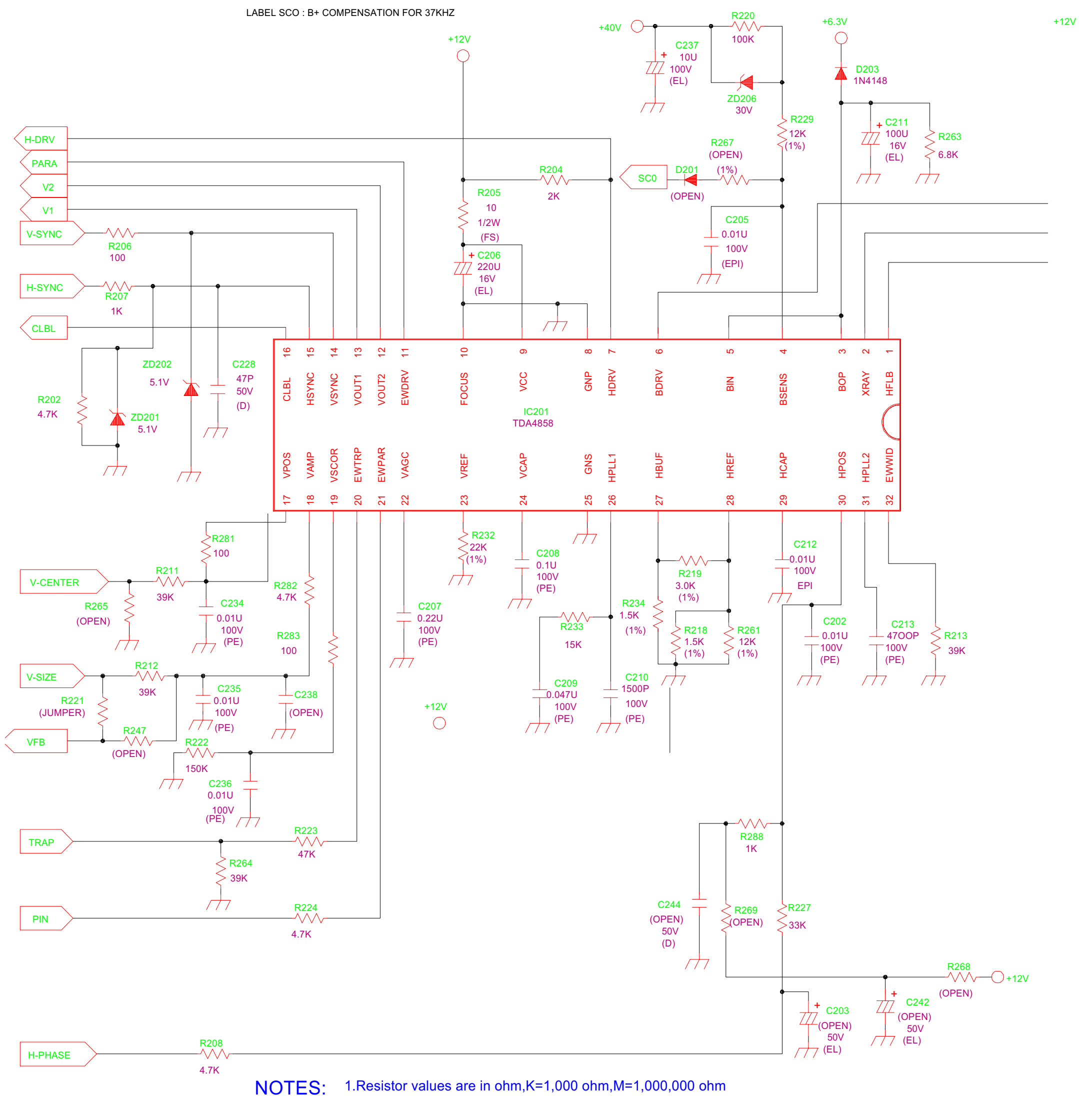


2.1.2 Autosync Deflection Controller--TDA4858

(a) Following form shows the TDA4858 pinning

SYMBOL	PIN	DESCRIPTION
HFLB	1	horizontal flyback input
XRAY	2	X-ray protection input
BOP	3	B+ control OTA output
BSENS	4	B+ control comparator input
BIN	5	B+ control OTA input
BDRV	6	B+ control driver output
HDRV	7	horizontal driver output
GNDP	8	ground (power ground)
Vcc	9	positive supply voltage
CLSEL	10	clamp select
EWDRV	11	EW parabola output
VOUT2	12	vertical output 2(ascending sawtooth)
VOUT1	13	vertical output 1(descending sawtooth)
VSYNC	14	vertical sync input / output
HSYNC	15	horizontal / composite sync input
CLBL	16	video clamping pulse / V-blanking output
VPOS	17	V-shift input
VAMP	18	V-size input
VSCOR	19	vertical S-correction input
EWTRP	20	EW trapezium correction input
EWPAR	21	EW parabola amplitude input
VAGC	22	external capacitor for V-amplitude control
VREF	23	external resistor for vertical oscillator
VCAP	24	external capacitor for vertical oscillator
GNDS	25	ground (signal ground)
HPLL1	26	external filter for PLL1
HBUF	27	buffered F/v voltage output
HREF	28	reference current for horizontal oscillator
HCAP	29	external capacitor for horizontal oscillator
HPOS	30	H-shift input
HPLL2	31	external filter for PLL2/soft start
EWWID	32	H-size input

(b) TDA4858 is an AutoSync Deflection Controller (ASDC).



(c) Pin 1 is AFC feedback.

(d) Pin 2 is an input of x-ray protection. If Vx-ray ≧ 6.38V, TDA4858 will shutdown.

(e) R220 and R229 are HV feedback resistors which can decide the horizontal B+.

(f) Pin 6 provide a B+ drive duty pulse. The duty pulse must be inverted by Q201,then send to step-up CKT.

(g) Pin 11 generate a parabola waveform for pin-cushion correction CKT.

(h) Pin 16 generate a clamp and V-blanking composite sync. for clamp CKT.

(i) Pin 17, 18, 20, 21 are V-center, V-size, Trapezoid, Pin-cushion DC control pins controlled by uc.

(j) The vertical free-run frequency is decided by C208, R232.

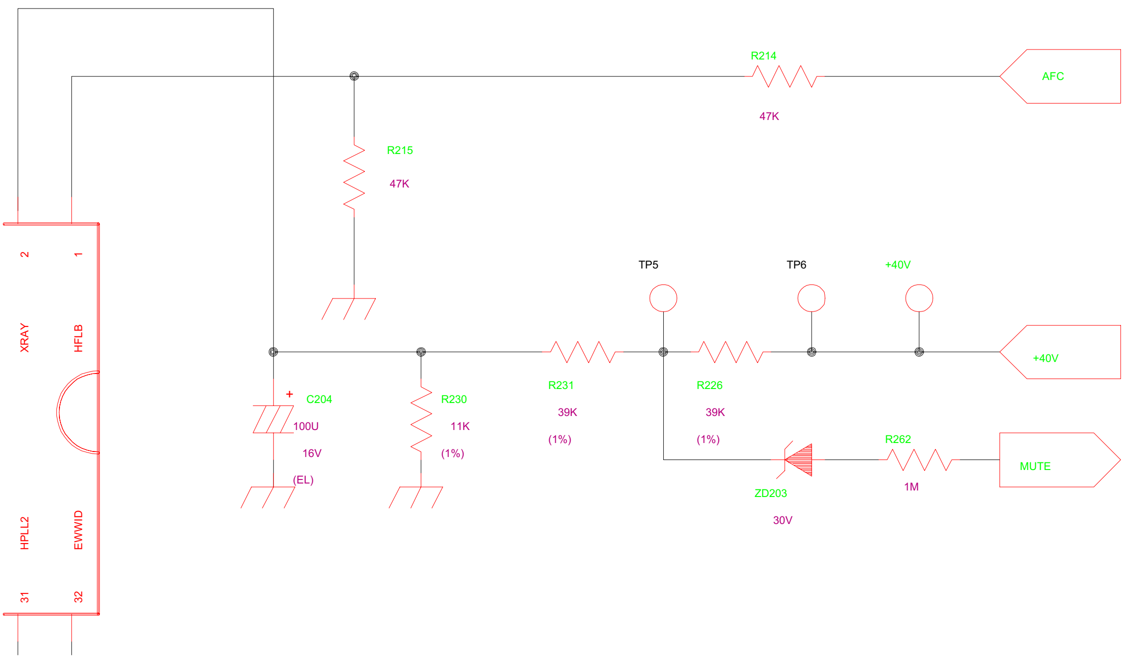
(k) The pin27 & pin28 setting the horizontal output frequency range (29KHz ~ 54KHz currently), and decided by R234, R219, R218, R261, and C212.

(l) Pin 31 PLL 2 provides soft star function when VPLL2 > 4.4V, TDA4858 active.

2.1.3 X-ray protection & AFC(Auto Frequency Control)

(a) AFC in other words is HFLB (Horizontal FLyBack) IC201 pin1, its for synchronize the second stage(horizontal deflection) with first stage (input signal H-sync.).

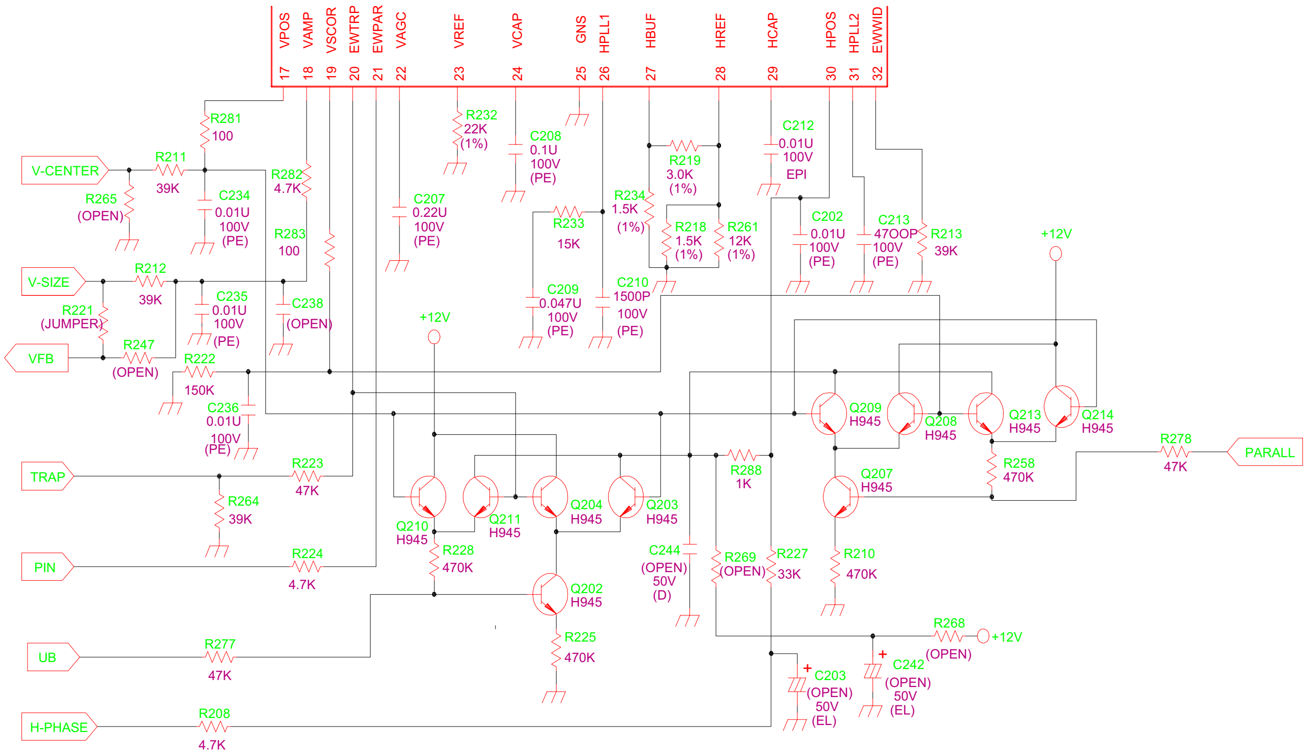
(b) TDA4858 pin2 sense the voltage separated by R226,R231 and R230 from FBT pin9 40V. The TDA 4858 pin2 trigger voltage is 6.38V. When the FBT pin9 40V increase to let the R230 voltage drop achieve 6.38V, the TDA4858 will shutdown. In the time H.V.=27.5KV.



2.1.4 Parallelogram circuit

(a) Q208, Q209, Q213. Q214 and Q207 construct the parallelogram control circuit.

(b) Q202, Q203, Q204, Q210 and Q211 construct the unbalance control circuit.



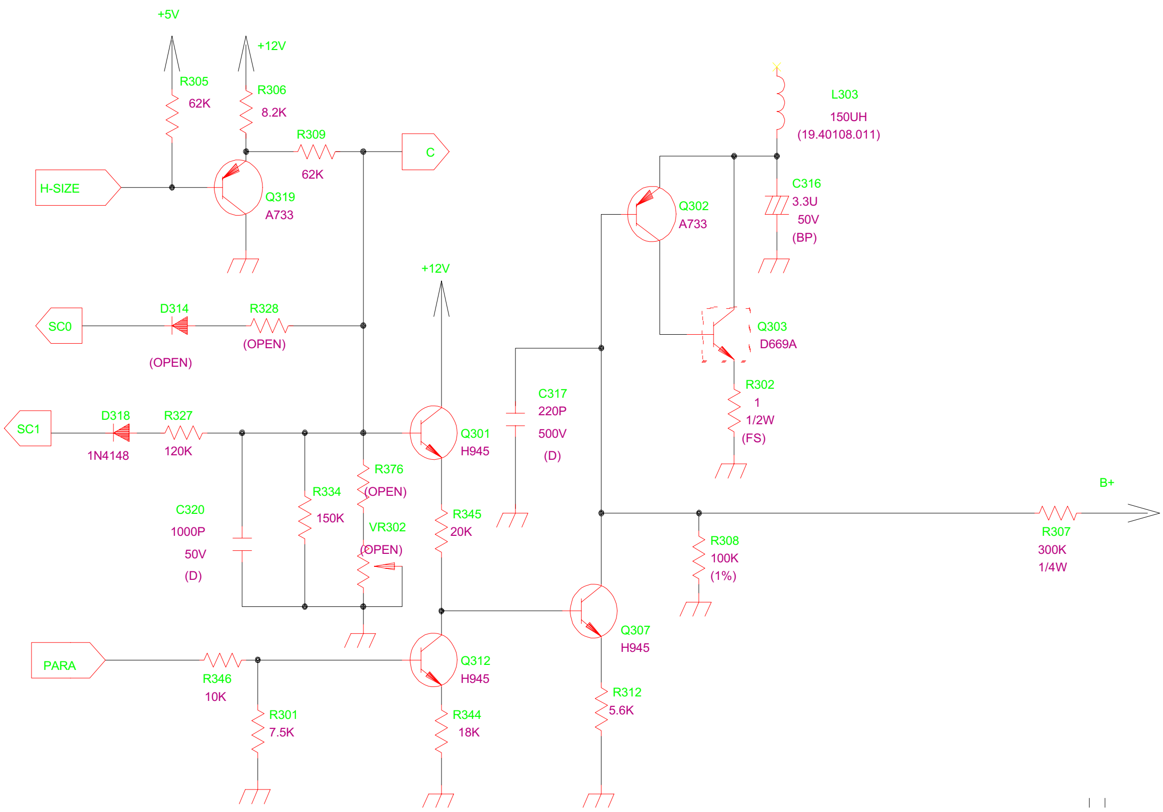
NOTES: 1.Resistor values are in ohm,K=1,000 ohm,M=1,000,000 ohm

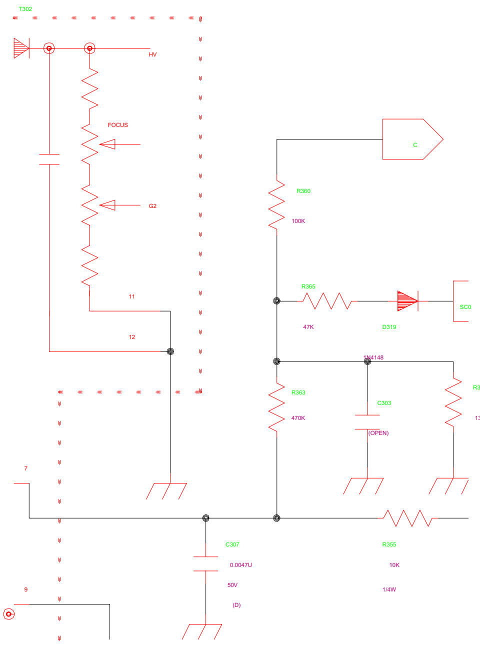
2.1.5 H-size Control Circuit

(a) H-size control voltage 0~5V input from "H-SIZE" net.
(b) Q319 is a buffer to separate prior signal and latter.
(c) R327 and D318 series connect to SC1 is used to compensating H-size by different horizontal frequency (for VGA) . The SC0,SC1 status are as follows:

Fh	SC0	SC1
>=42KHz	1	1
42 ~ 37KHz	0	1
<37KHz	0	0

SC truth table





(d) Horizontal size module merge the side-pin compensation waveform coming from Q312 then through Q307 inverting-amplify the modulating wave to control Q302、Q303 Darlington pair to control H-size.

(e) Due to the VGA H-size range is too large to limit by SC0~SC1, it need a extra limit circuit for VGA mode. R356, R359, R357, R358 and Q322 construct the limit circuit when SC0 and SC1 is "LOW" simultaneously.

(f) R363, R364 and R360 is horizontal regulation compensation circuit, R365 and D319 series connecting to SC0 for Fh < 37KHz to reduce the compensation quantum.

(g) R307 and R308 separate the voltage B+ then provide the different voltage for different horizontal frequency to H-size modulation circuit.

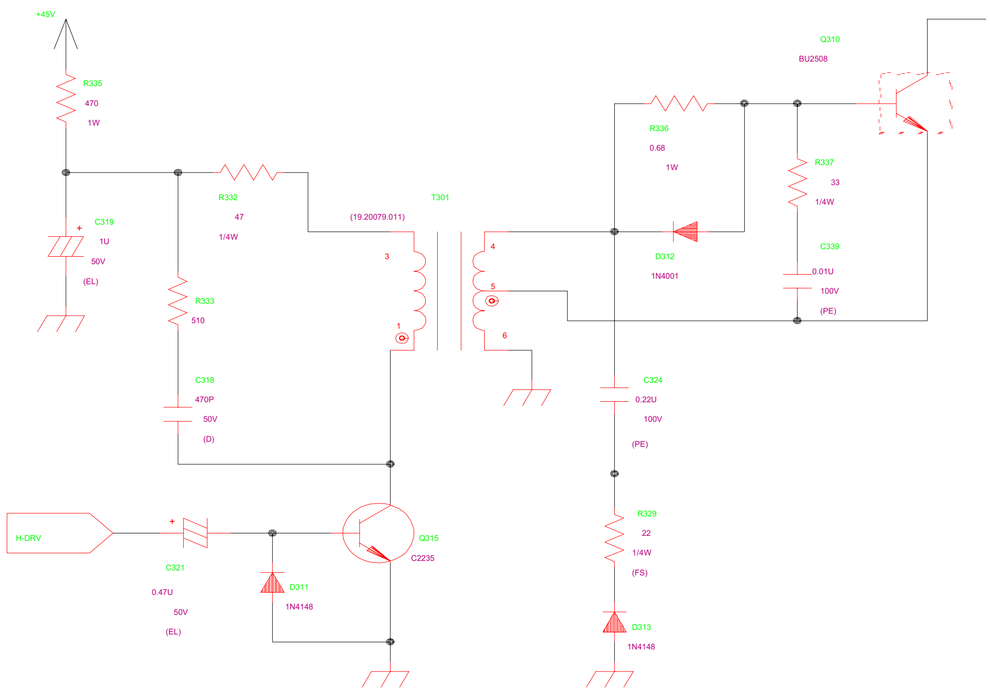
2.1.6 Horizontal output circuit

(a) C321 couple the HDRV wave form from TDA4858 pin7 to Q315 for switching signal and get the energy by R335 and R332 series, then through the driver transformer T301 couple the driver wave form to horizontal transistor Q310 via R336 at plus duty and via D312 at minus duty.

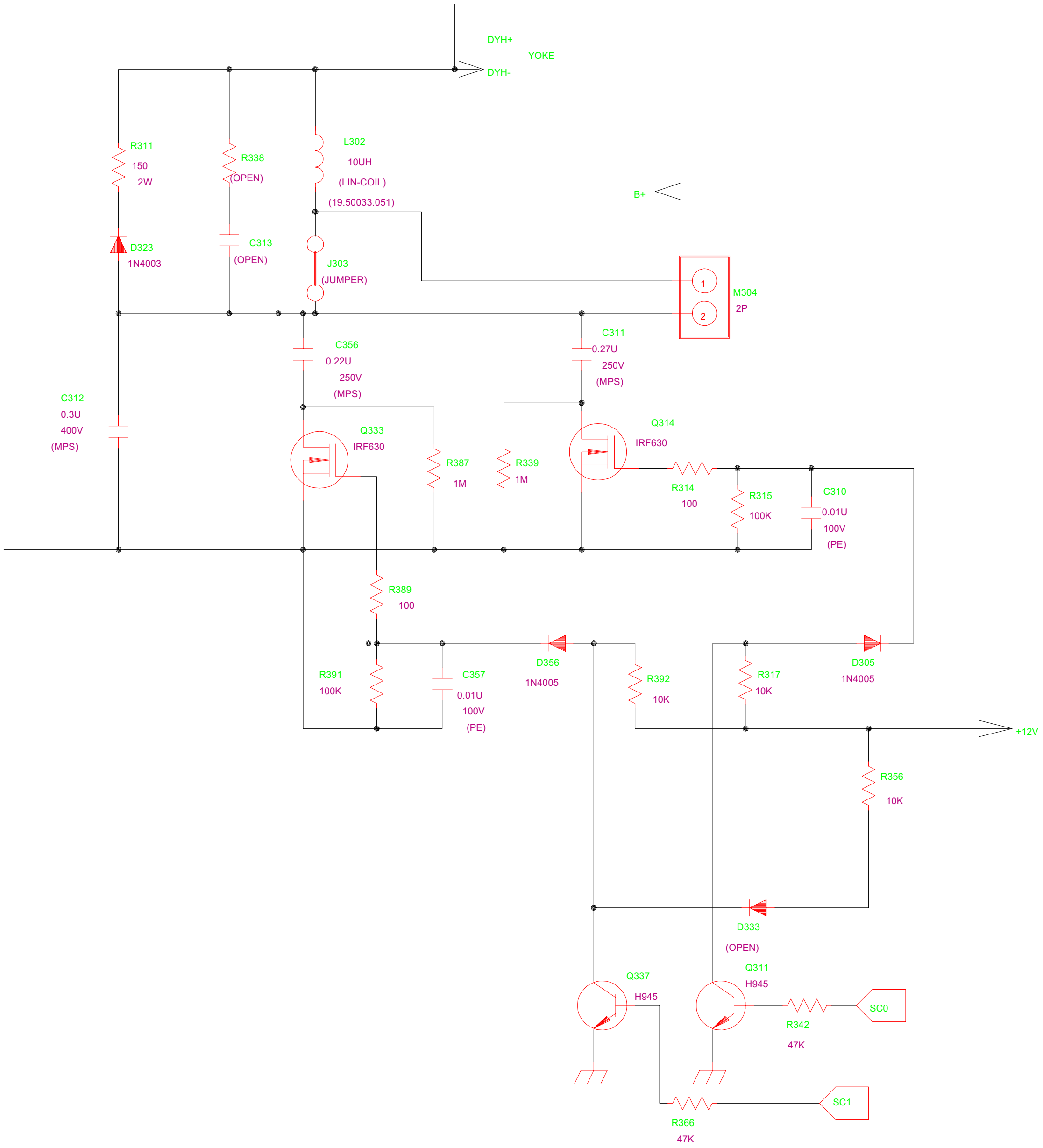
(b) While the horizontal transistor Q310 switching a cycle, the energy provided from FBT T302 pin6 B+ be stored in horizontal deflection yoke and tunning capacitor C314. The deflection sawtooth current through horizontal deflection yoke was generated during the Q310 at ON cycle provides the plus part and during Q310 at latter OFF cycle provides the minus part through the flyback diode D307.

(c) R333 and C318 series is a snubber circuit to inhibit spike.

(d) C324, R329, D313 and D310 is used to compensate the cross-over distortion when the D307 OFF Q310 ON.



2.1.7 H-Linear correction circuit



(a) L302 is Linear coil for linearity correction and C312 is Cs capacitor for deflection current S correction.

(b) R338 and C313 series that parallel to L302 pin1-2 for ringing inhibit. The goal of R311 and D323 series is both dismissing ringing bar and good linearity.

(c) Reference to SC truth table, Fh>42KHz Cs = C312.And Fh<42KHz,then Cs = C311 parallel to C312

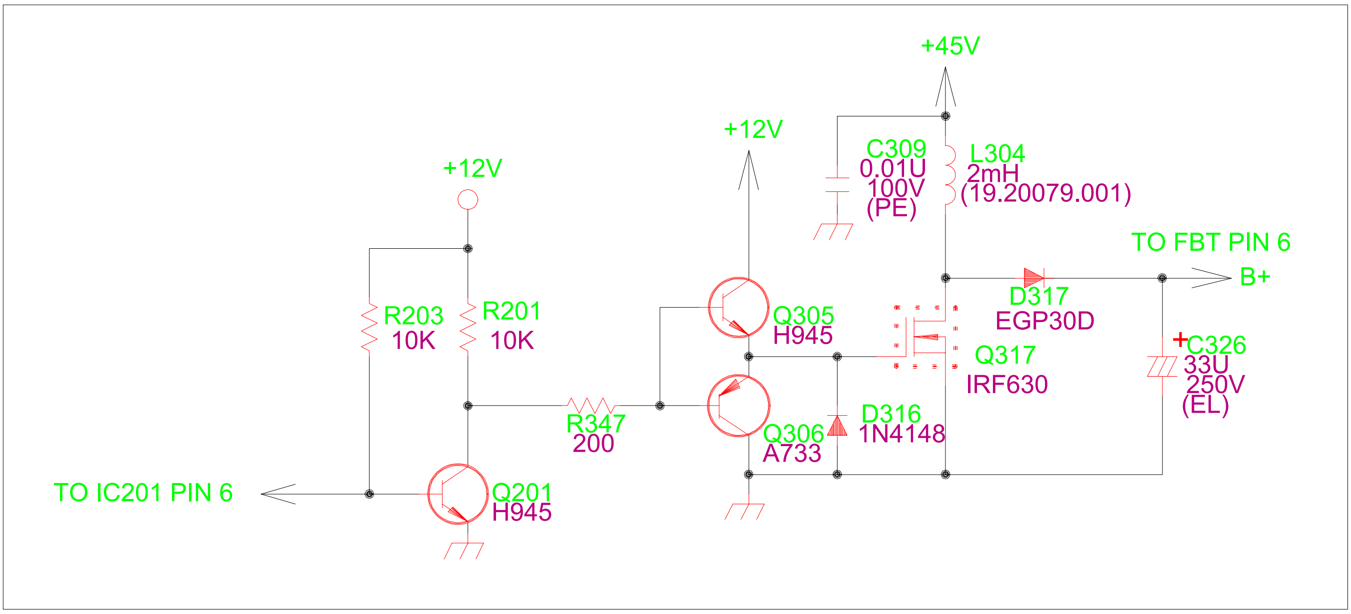
2.1.8 Step-up CKT

(a) B^{+}drive duty pulse comes from TDA4858 pin 7

(b) Q305, Q306 constructed class B output to drive Q317.

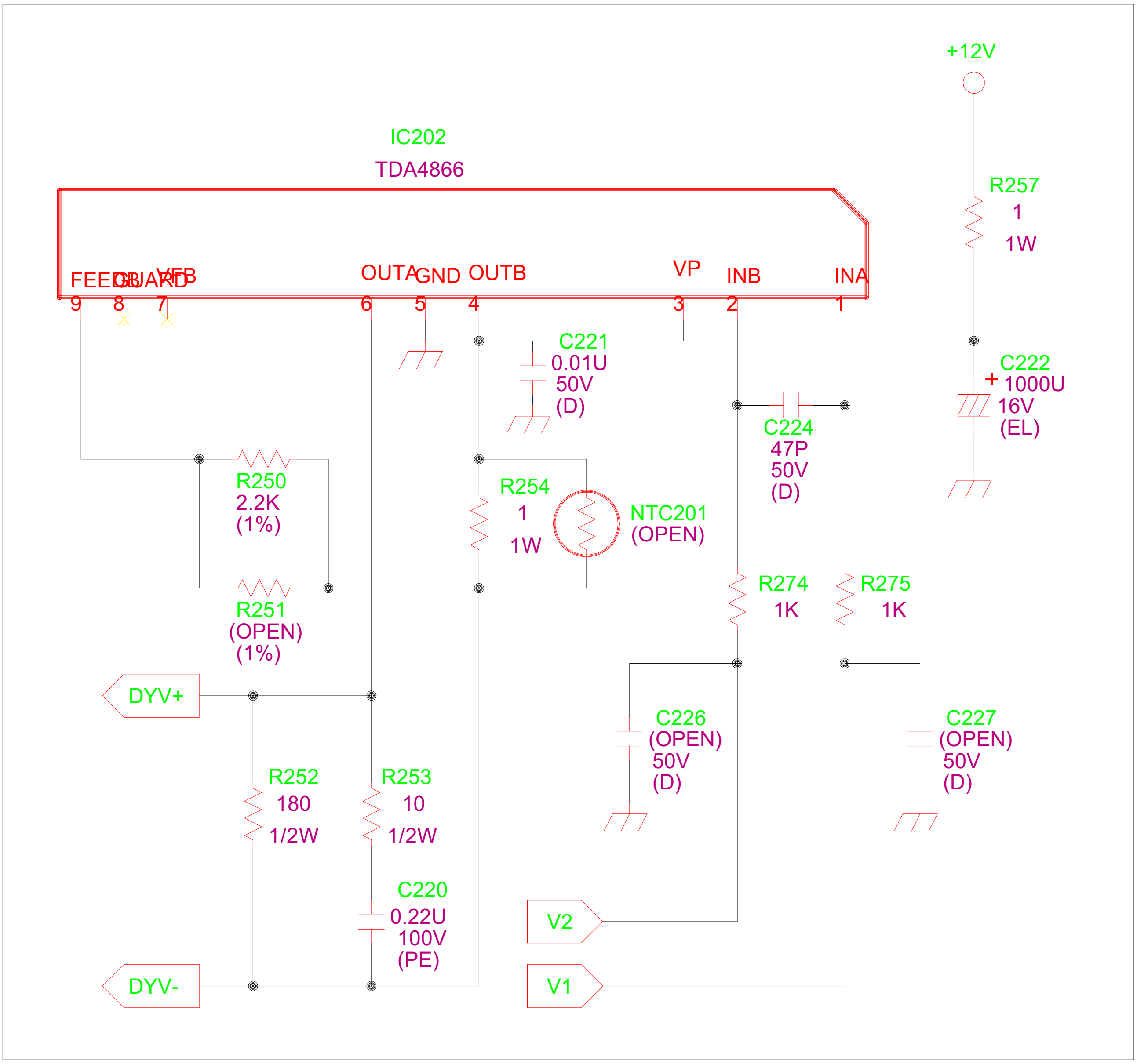
(c) When Q317 turns on, L304 storage energy and D317 is off. when Q317 turns off L304 release energy and D317 turns on to charge C326 to B+

(d) The higher Hor. frequency needs higher B^{+} so B^{+}Drive duty must vary with frequency.



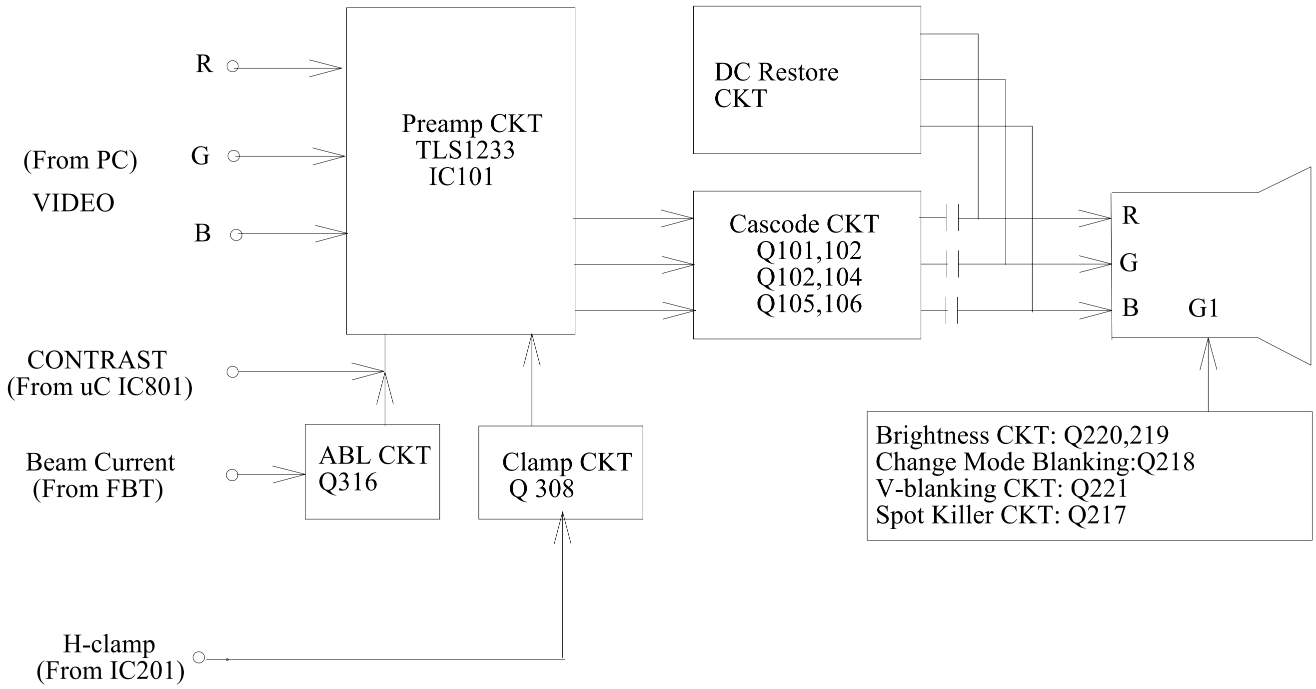
2.1.9 Vertical output

(a) TDA4866 is a vertical deflection amplifier, pin7 need a higher DC voltage(45V currently) for deflection current amplify.
(b) TDA4866 pin1,2 is vertical drive input pin from TDA4858 pin12,13.
(c) Pin 4,6 is vertical deflection output pin to drive vertical YOKE.
(d) Pin8 provides the vertical blank signal for vertical retrace line canceling.



2.2 Video CKT

2.2.1 Black Diagram of Video



2.2.2 TLS1233 Block Diagram

The function block below represents one of the threevideo amplifiers in the TLS1233 along with the contrast , gain adjust and brightness contrals. The Contrast Control is DC-Level (0 ~ 4 V) operate attenuator which controls the video gains of the three channels (R ,G ,B)simultaneously The Gain Adjust Control, which is also a DC-level operated circuit, provides a 6 Db gain adjustment to each channel. During the retrace period ,the Clamp Comparator will charge or discharge the clamp capacitor by comparing the external brightness (clamp+) level with the video output DC level thus that the brightness level is maintained.

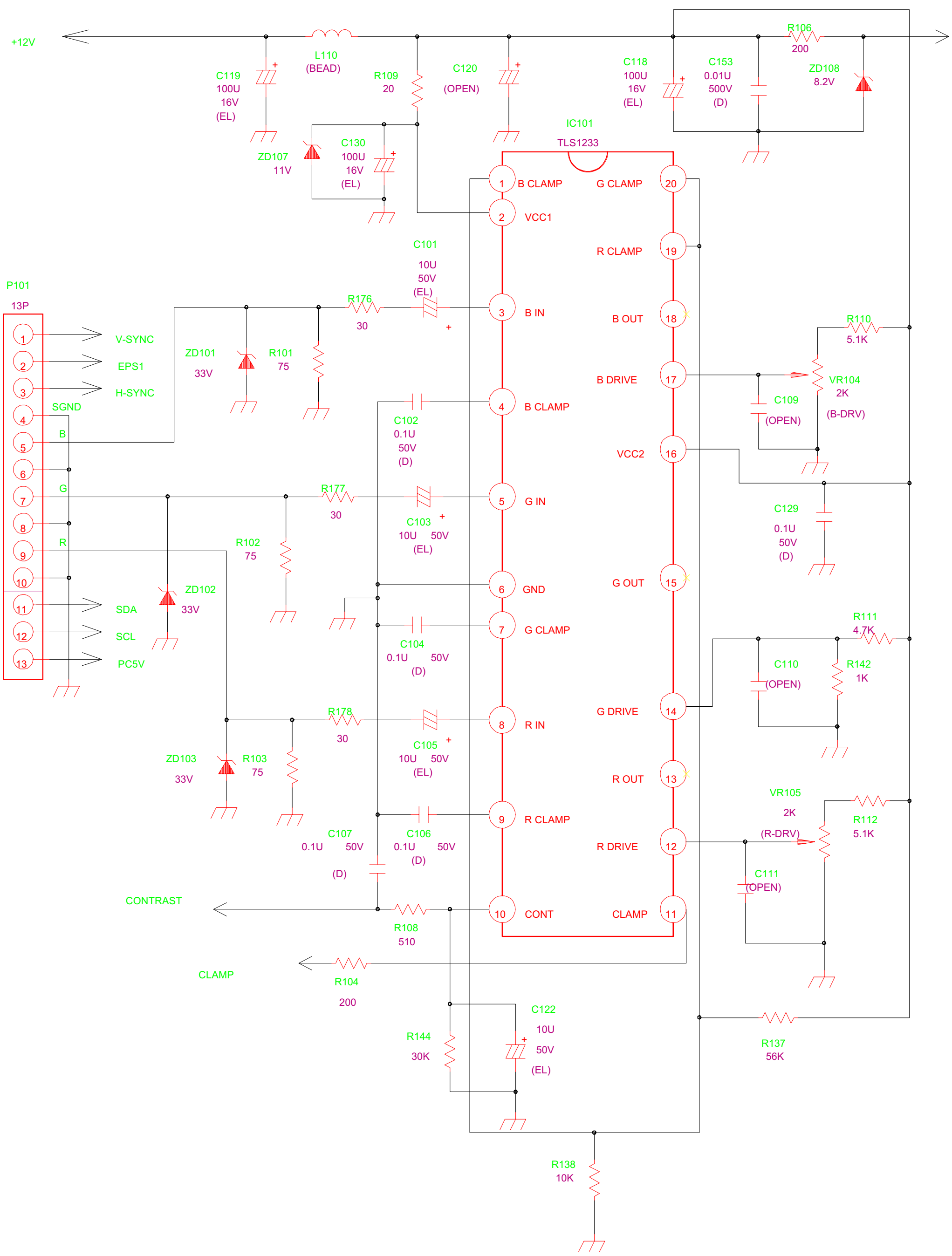
2.2.3 Preamp CKT

(a) AS shown in the block diagram:
The R/G/B signals will generate an enough amplitude of Vpp to show up on the CRT screen after the amplification of the amplifiers.

(b) The purpose of signal CLAMP is to fix the black level of all R.G.B signals to the same level after the AC couple. This is the DC Restoration of pre-amplify

(c) To fix Pin 1,19,20 voltage is to stabilize Pin 13,15,18 (R,G,B Output) DC voltage.
It's purpose is to lower the Temp. of IC and transistors of Casecode CKT.

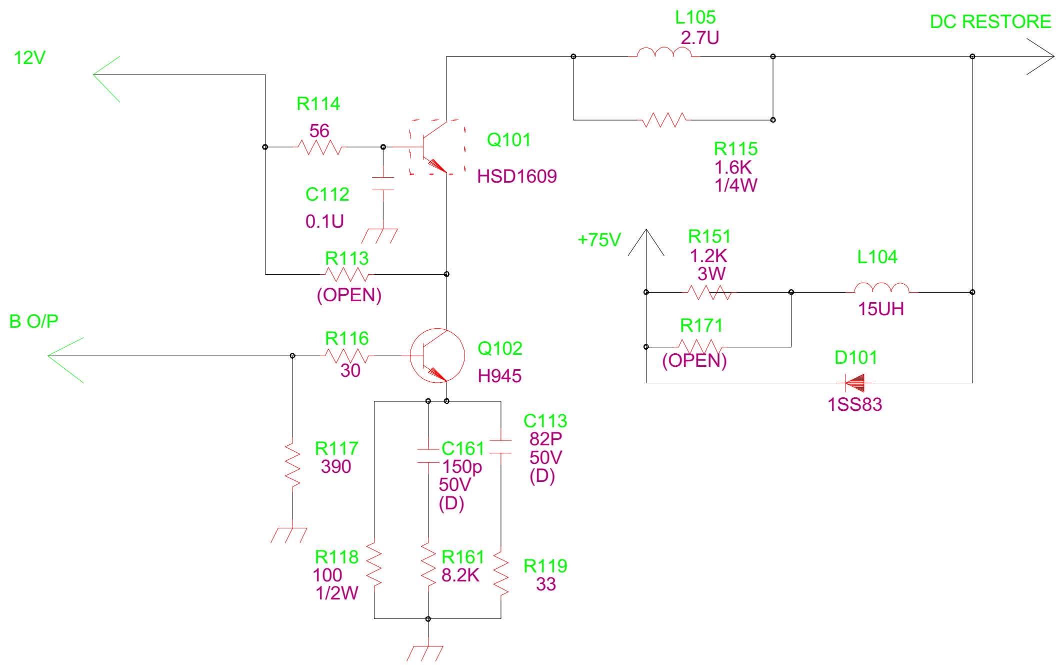
(d) VR104,105 control R.,G O/P gains



2.2.4 Cascode CKT

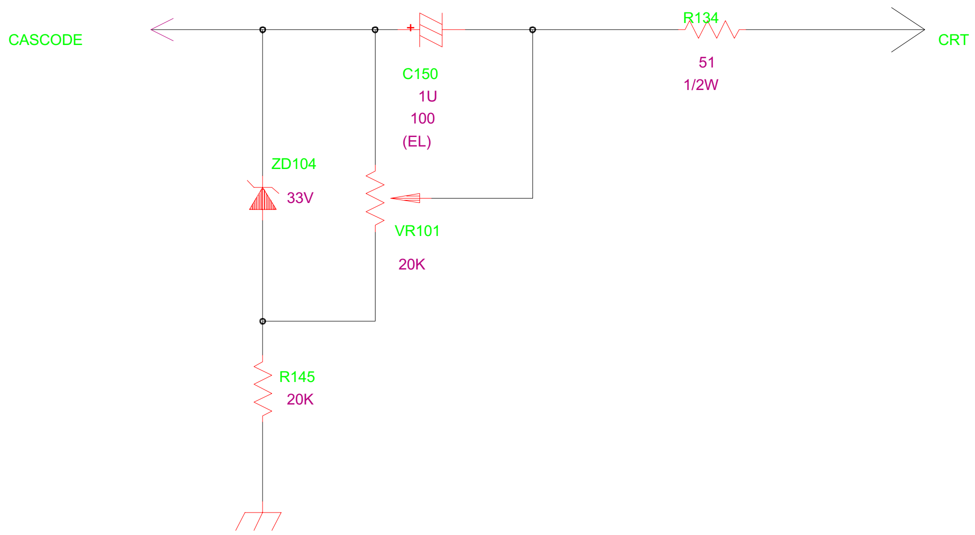
(a) Output stage adopts cascode circuit Its purpose is to amplify the signal which has been processed by TLS1233 to a enough amplitude of Vpp, then display on the CRT. The criteria to select a cascode transistor is the smaller the value of Cob and the bigger the value of Ft is better .This circuit adopts HSD1609. Cob=3.8pF, ft=140MHZ.

(b) Cascode CKT concludes 3 band amplification.
Mean Freq.: capacitance open, inductance short. The gain = Rc /Re
High Freq.: (R gun),peaking coil L104,L105,R115,C113,R119
Over Freq. Compensation: (R gun),C161,R161.



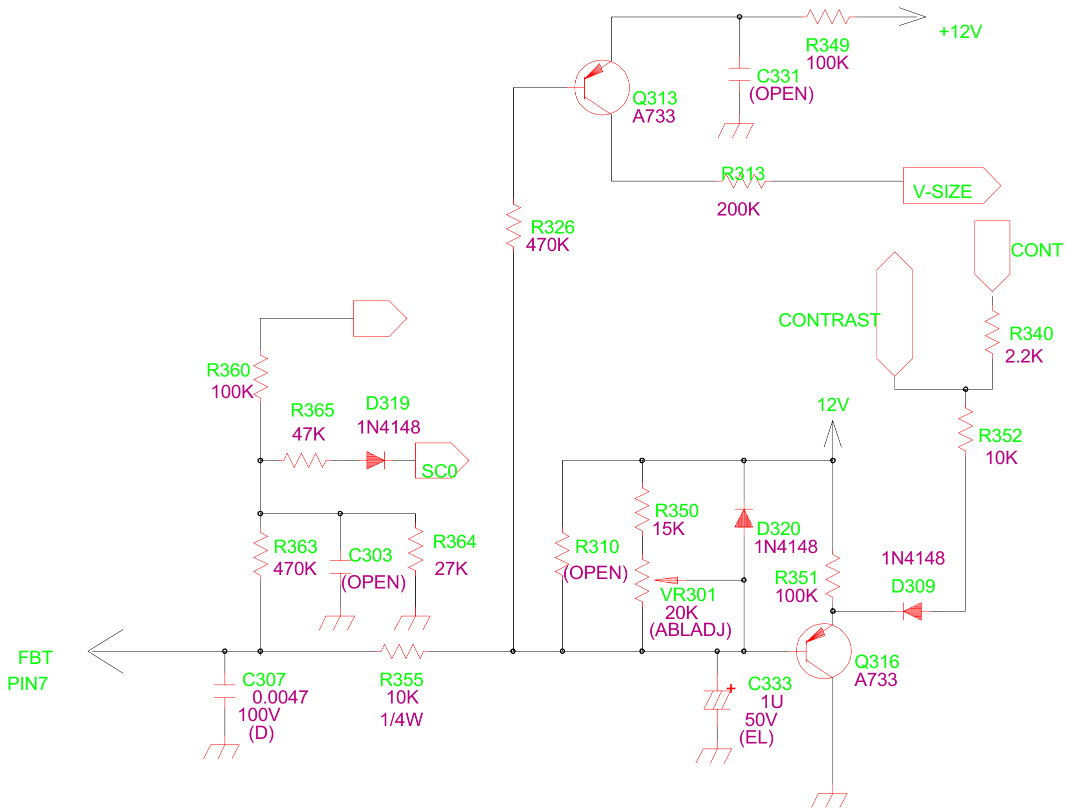
2.2.5 DC Restore CKT:

(a) The video signal amplified by the output stage is coupled to CRT by way of AC coupling. So DC restoration CKT is needed to do the white balance adjustment.
(b) Use VR101 & R145 and ZD104 to get the range of each gun bias (Max ≒ 27 V).
(c) O/P signal mixes DC and AC voltage. Only AC signal passes C150. DC voltage is generated by VR101 cross voltage.



2.2.6 ABL CKT (Auto Brightness Limit)

ABL is a protection circuit. When the anode current goes higher than the setting value of ABL circuit . ABL will pull down the voltage of contrast to limit the anode current. This is helpful to protect CRT.



a) With crosshatch patter, FBT beam current is smaller. It makes the voltage of C333 higher than Vcontrast Q316,is OFF the Vconstrast is freely controlled.

b) With the full white , FBT beam current rises, the voltage of C333 is down. It makes Q316 ON. Vce of Q316 is fixed

2.2.7 Brightness, V-blank, change mode blank, spot killer CKT

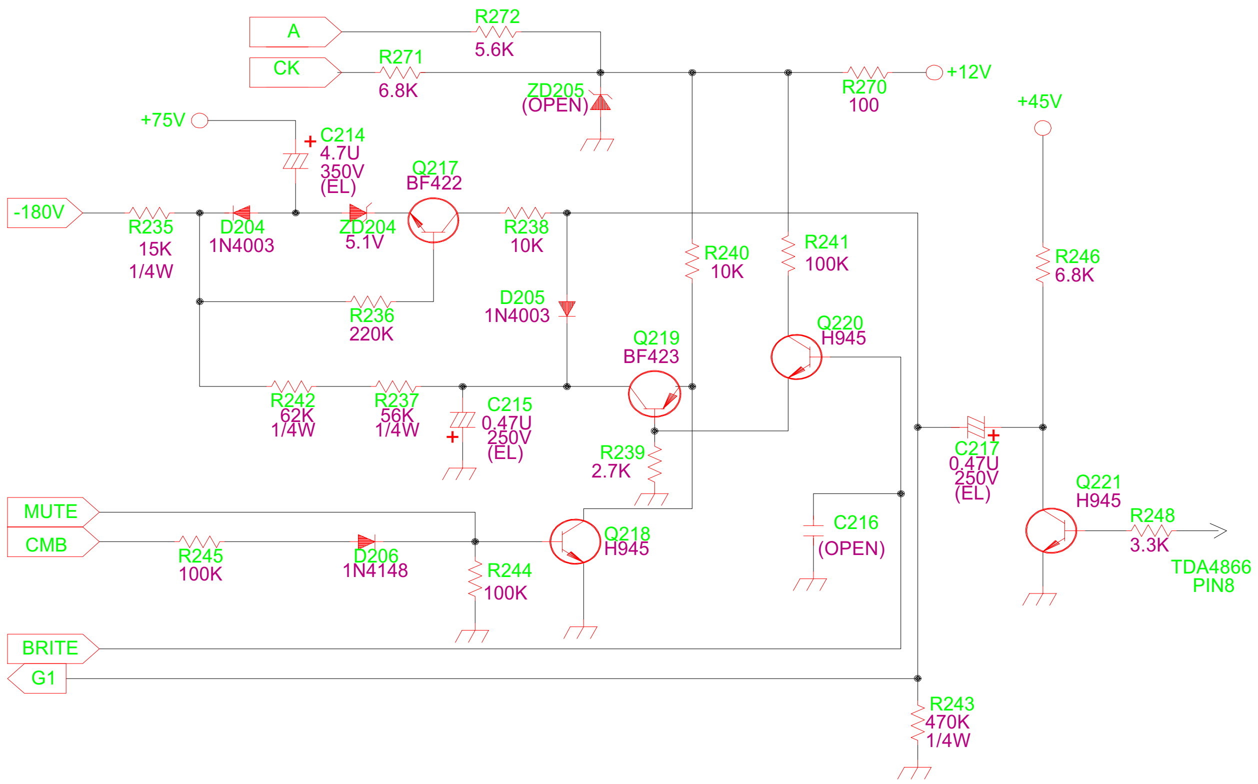
(a) About the cut off voltage, while the voltage, cathode to G1, over the cut off voltage, the picture will disappear. If the cut off voltage of the CRT G Gun is set at 110V and the black level of cathode is 60v, the picture want to show the signals higher the black level once the G1 voltage is lower than -50V.

(b) As described above, we may using the voltage control G1 as the brightness control. Generally the G1 control range is about 10~15V if the Raster brightness is from 0 to 1.5ft-L.

(c) Similarly, we may overlap a negative pulse of vertical duration on the G1 voltage to prevent the vertical retrace line from showing on the picture. This is to keep the voltage cathode to G1 over the cut off voltage during the period of vertical retrace.

(d) In order to prevent the picture occurred transiently while change mode, pull down the G1 voltage and let the voltage cathode to G1 over CUT OFF voltage. This will make the picture blanking

(e) While monitor turned off, the discharge speed of high voltage circuit is slow since there is no deflection scanning , a spot which will destroy the phosphor of CRT will display on the CKT. So the SPOT KILLER circuit will generate a negative voltage higher than CUT OFF to the G1 to cut the beam This is to protect the CRT.



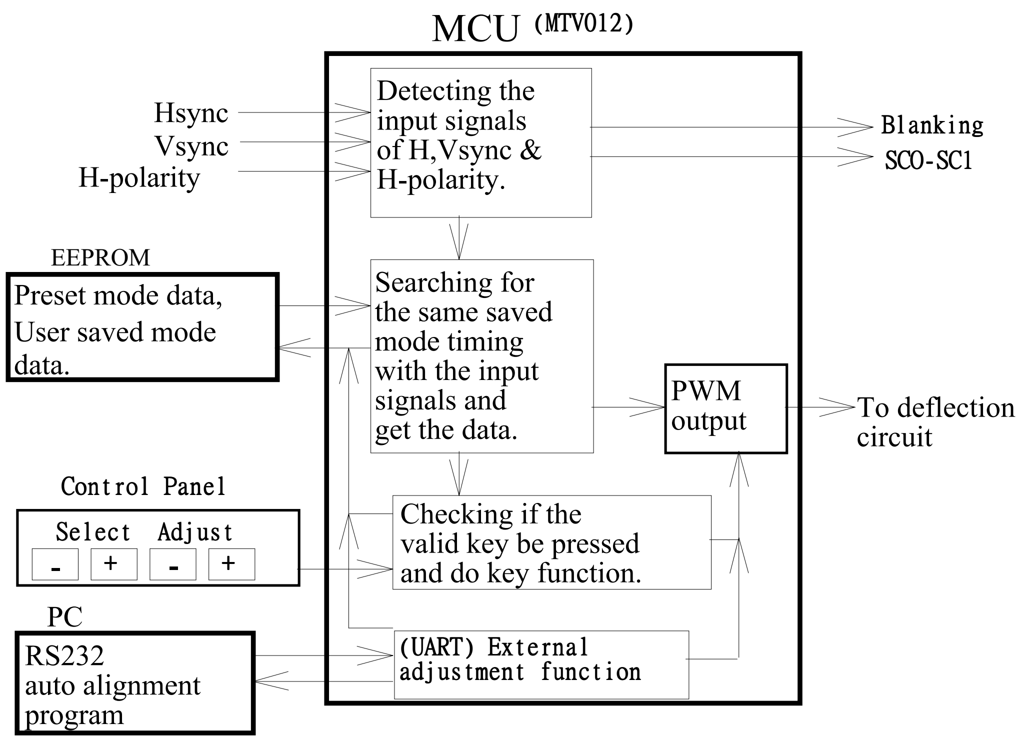
2.3 Micro Controller Circuit Operation Theory

2.3.1 Introduction

The microcontroller of the V551 can discriminate the display mode by detecting the frequency of the H/V sync signals and the polarity of horizontal sync signal. It provides DC voltages to control the picture and save the adjusted parameters into the EEPROM by using the control panel.

2.3.2 Block diagram

The major parts of V551 microcontroller circuit are MCU, EEPROM. The circuit block diagram is shown as below,



2.3.3 MCU

The MCU - MTV012 is an 87C51 microcontroller with PWM outputs. It manages the following functions,

(1) To detect mode and output proper SC0 and SC1 to deflection circuit.

(2) To check if there is the same saved mode in the EEPROM and get the data to transfer into DC voltages by PWM output and RC filter circuits to control the picture, contrast and brightness.

(3) To check if there is the valid key be pressed and do the key function.

(4) To memorize mode timings and any adjustable parameters of the picture into EEPROM.

(5) The inner registers and PWM output of MCU can be controlled by the external PC alignment program.

2.3.4 How to detect mode timing

Only when the mode timing input is stable, we can adjust the picture by the control panel, and the major measurement of the mode timing inputs are horizontal and vertical sync.

(1) Vertical sync frequency measurement:

We use the base timer, it can generate a count during a fixed time, this fixed time is 12/12MHz and we call it "Time base", so when the first vertical sync generated, we enable the base timer, and the next vertical sync generated, we disable the base timer, and we only need to calculate how many counts are during a vertical sync period.

The formula is

Vertical sync frequency

= FV

= 1 / Vertical sync period

= 1 / [Counts * (Time base)]

==> **Vertical sync frequency = 1000000 / Counts**

(2) Horizontal sync frequency measurement:

We use the event counter for calculating how many counts are during a long fixed time, because the vertical sync period is longer than the horizontal sync period, we can enable the event counter when the first vertical sync generated and disable the event counter when the next vertical sync generated, this time, we can get the horizontal sync counts during a vertical sync period.

The formula is

Horizontal sync frequency

= FH

= Horizontal sync counts / Vertical sync period

==> **Horizontal sync frequency**

= Horizontal sync Counts / Vertical sync period

2.3.5 What are the valid key functions for user

Total 4 keys for 7254e control panel, "select +" & "select -" are the selection of controlled function with LED change, and "adjust +" & "adjust -" are the selected item to increase & decrease volume.

Except the last basic key functions, the user can press "select +" & "adjust -" to recall the factory preset data. Meanwhile it takes about 20 seconds for keeping no key pressed to store the adjusted function into the user data.

2.3.6 How to execute the auto alignment function

The MCU supports the UART function, it has 2 I/O ports, one is the receiver, the other is the transmitter, they are connected with an interface to PC and PC can execute alignment program by RS232 communication to send the formatted data to the MCU for adjusting any adjustable parameters of the picture and saving the adjusted values into EEPROM. By this way, we can get the products with the same quality and reduce the manufacturing time.

2.4 Power Supply Circuit Operation Theory

2.4.1 Brief

Acer V551 is equipped with a current mode, constant frequency, synchronous, using fly back switching mode power supply circuit,(The operating frequency won't vary with the change of input voltage or output load. This means synchronous with monitor .) In abbrev, the SMPS or SPS.

Input : 90VAC - 264V AC (full range)

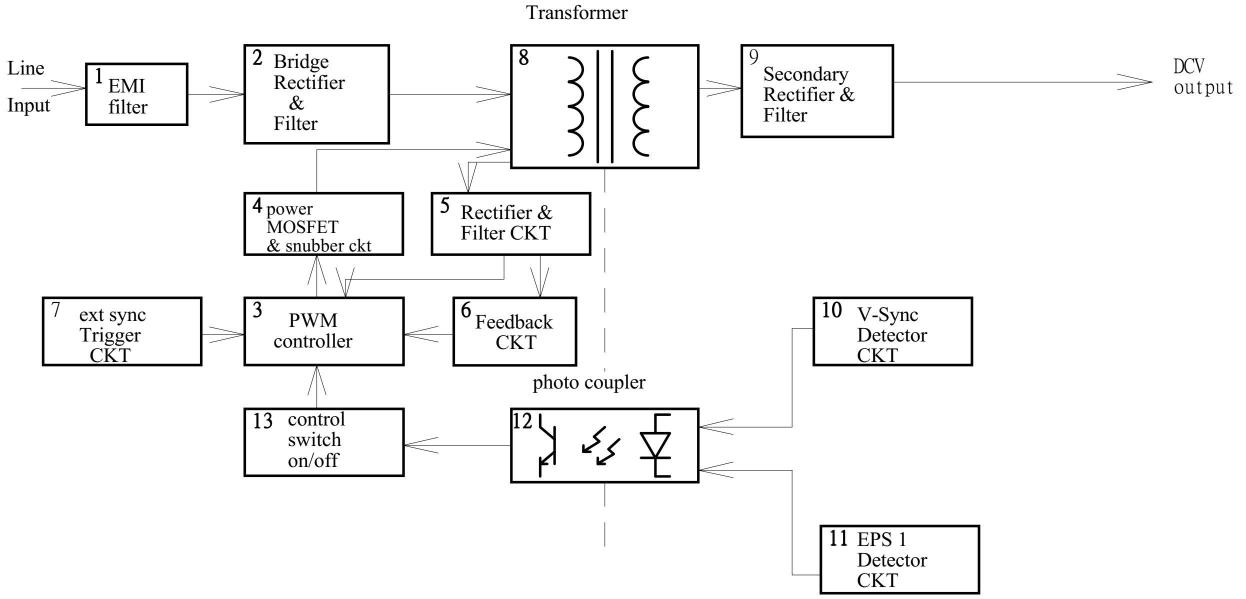
Output :	+43.5V	0.9A	39.15W
	+75V	0.07A	5.25W
	+12V	0.76A	9.12W
	+ 6.5V	0.6A	3.9 W

Total output power : 57.42w

2.4.2 Circuit Analysis

The block diagram is shown as follow , is divided into 13 portions

2.4.2.1 Block Diagram



1. EMI filter CKT
2. Power SW & Rectifier, filter CKT
3. PWM controller
4. Power Mosfet & Snubber CKT
5. Rectifier & Filter CKT
6. Feedback CKT
7. Sync. CKT
8. Transformer
9. 10-12: Rectifier & Filter CKT
10. V-sync Detector CKT
11. EPS1 Detector CKT
12. Photo coupler
13. Control switch on/off

1. EMI filter CKT is a necessary circuit for restraining the electromagnetic interference to meet the standard of FCC and FTZ. This portion of circuit comprised capacitor, Y capacitor, common mode choke, differential choke, etc.

2. Power SW and rectifier filter CKT:
Power SW is used for the control of power on and off Rectifier Filter is able to process the input AC voltage into a DC voltage, This circuit is designed to operate normally form 90V to 264V AC. This is so called full rage or universal input.

3. PWM control IC

UC3842 is a current mode of PWM control IC. Please refer to the attachment A to see the specification. Because the saw wave and feedback control is separated, it is ideal for the synchronous operation of the SPS of multi-frequency monitor.

Some PWM IC combines the saw wave and feedback control as one is not good for the synchronous operation of multi-frequency monitor's SPS circuit. It happens the on-off transistor (or MOSFET) destroyed during the horizontal frequency is switching. That's the reason we adopt UC3842 as the control IC.

* When load changes, the voltage of the primary coil (pin 6-7) of the transformer will be rectified and filtered by D608, C608, D607,C607. This voltage value will go down while the load getting heavier and it's voltage will be divided via R616,VR601,R617 then entering pin 2 of C601 (Verror is direct ratio of output load).

This signal is compared with primary current to decide the amplitude of duty cycle. When output load gets heavier, the time period of power MOSFET turns on will get longer and vice versa. This principle is used to control the output voltage stablely, As described above, the current mode CKT has a dual feedback, one is from the variation of output load, the other is from the variation of primary current, This causes the response to the variation of AC source voltage, i.e. a good line regulation.

The function of R613, C615 is to generate a oscillation frequency being the clock input of UC3842, R614, C617, D611, D612 is a soft start circuit to assure a proper ON time as the monitor turns on to prevent from the MOSFET destroyed by the surge current the principle is UC3842 won't work while pin 1 of UC3842 is low. Please check **attachment A.**

Besides, the operating voltage of UC3842 is 16V while start and 10V after start. In this circuit, the start voltage is provided by R602, R603. The C607, T601 will work after start and the auxiliary coil (pin 8-9) of T601 will generate a voltage to be rectified and filtered by C608, D608, D607,C607 to maintain the operation.

4. Switching FET & Snubber circuit.

   Switching FET is mainly used for the operation of on and off. It is controlled by IC601.We can obtain the result of FET turn on and off. Snnbber circuit is mainly consisted of C624, R619, D614, D610, R604 and C613. It's purpose is to restrain the turn off voltage spike of FET. To prevent it from destroying for Q602.

5. Rectifier and filter CKT comprises D608,C608,D607,C607 to provide the Vcc for IC601.

6. Feed back CKT comprises R616,VR601,R617 is mainly to divide the voltage of primary auxiliary coil, then enter pin 2 of 3842 and compare with the internal Vref (2.5V) of IC601 to obtain a stable output voltage.

7. SYNC. CKT

   In order to prevent from the interference on the picture caused by the difference of the oscillation frequency of SPS and the horizontal scan frequency of monitor , We use SYNC. CKT to unify these two frequency. This CKT is consisted of C616,ZD603,R612 and detect the synchronous

signal from the monitor FBT core. After the differential of C616,ZD603 clips it's voltage. And then add this signal to the pin 4 of UC3842 by way of 612 and C615 to get the synchronous.

8. Transformer is mainly used for transformer and isolation it's principle is the current will pass pin 1-4 of T601 when FET on and energy being output by T601 when FET off.

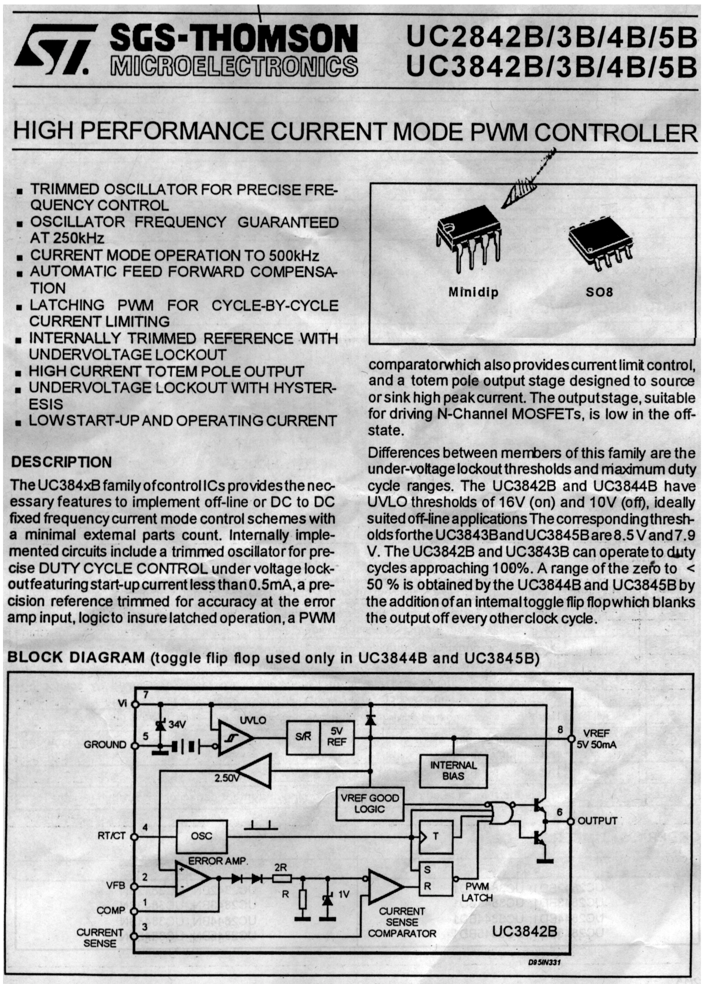
9. 10-12:This + 43.5V of Rectifier and filter CKT is consisted of D702,C703 and the other groups of output voltage is using the same principle to do the rectifier and filtering

10. The V-sync is low or full high, then IC602 is not drived.
The V-sync is pulse, then the waveform of Q701 collector is sharp pulse.

11. When the ESP1 is floating, The IC602 is always drived. At the same time there is not power saving function. When the ESP1 is Ground, then the IC602 drived according to V-sync.

12. The photo coupler adopts TLP721F of Toshiba and main purpose is that the primary and secondary is isolated.

13. When V-sync is inactive, IC602 is not drived, Q603,Q604,Q605, turn on.Q602 turn off. The power shut down and the monitor is in off mode. When V-sync is active . IC 602 is drived. Q603, Q604, Q605 turn off. Q602 turn on and the monitor in normal mode.


SGS-THOMSON MICROELECTRONICS

UC2842B/3B/4B/5B
UC3842B/3B/4B/5B

HIGH PERFORMANCE CURRENT MODE PWM CONTROLLER

- TRIMMED OSCILLATOR FOR PRECISE FREQUENCY CONTROL
- OSCILLATOR FREQUENCY GUARANTEED AT 250kHz
- CURRENT MODE OPERATION TO 500kHz
- AUTOMATIC FEED FORWARD COMPENSATION
- LATCHING PWM FOR CYCLE-BY-CYCLE CURRENT LIMITING
- INTERNALLY TRIMMED REFERENCE WITH UNDERVOLTAGE LOCKOUT
- HIGH CURRENT TOTEM POLE OUTPUT
- UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LOW START-UP AND OPERATING CURRENT

Minidip   SO8

DESCRIPTION

The UC384xB family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include a trimmed oscillator for precise DUTY CYCLE CONTROL under voltage lockout featuring start-up current less than 0.5mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC3842B and UC3844B have UVLO thresholds of 16V (on) and 10V (off), ideally suited off-line applications The corresponding thresholds for the UC3843B and UC3845B are 8.5 V and 7.9 V. The UC3842B and UC3843B can operate to duty cycles approaching 100%. A range of the zero to < 50 % is obtained by the UC3844B and UC3845B by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

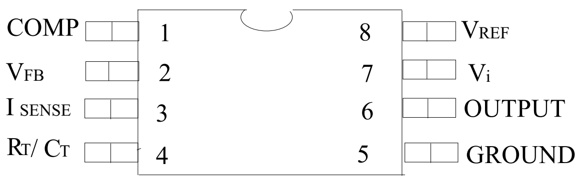
BLOCK DIAGRAM (toggle flip flop used only in UC3844B and UC3845B)

Symbol	Parameter	Value	Unit
Vi	Supply Voltage (low impedance source)	30	V
Vi	Supply Voltage (li < 30mA)	self limiting	
Io	Ouptut Current	±1	A
Eo	Output Energy (capacitive load)	5	μJ
	Analog imputs(pins 2,3)	-0.3 to 55	V
	Error Amplifier Output Sink Current	10	mA
Ptot	Power Dissipation at Tamb ≦ 25℃ (Minidip)	1.25	W
Ptot	Power Dissipation at Tamb ≦ 25℃ (SO8)	800	mW
Tstg	Storage Temperature Range	-65 to 150	℃
TL	Lead Temperature (soldering 10s)	300	℃

* All voltag ges are with respect to pin 5, all currents are positive into the specified terminal.

PIN CONNECTION (top view)

Minidip/SO8



D95IN332

PIN FUNCTIONS

NO	Function	Description
1	COMP	This pin is the Error Amplifier output and is made available for loop compensation.
2	VFB	This is the inverting input of the Error Amplifier, It is normally connected to the switchingt power supply output through a resistor divider.
3	ISENSE	Avoltage proportional to inductor current is connected to this input. The PWN uses this information to terminate the output switch conduction.
4	RT/CT	The oscillator frequency and maximum output duty cycle are programmed by connecting resistor RT to Vref and cpacitor CT to ground. Operation to 500KHZ is possible.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET.Peak currents up to 1A are sourced and sunk by this pin.
7	Vcc	This pin is the positive supply of the control IC.
8	Vref	This is the reference ouptput. It provides charging current for capacitor CTthrough resistor. RT.

ORDERING NUMBERS

SO8	Minidip
UC2842BD1; UC3842BD1	UC2842BN;UC3842BM
UC2843BD1; UC3842BD1	UC2843BN;UC3843BM
UC2844BD1; UC3842BD1	UC2844BN;UC3844BM
UC2845BD1; UC3842BD1	UC2845BN;UC3845BM

Table of Contents

V551 Alignment Procedure

3.0 Preparation for Alignment

a. Pre-set all VRs to the center position except R/G/B bias VR101, 102, 103 counterclockwise to maximum.
b. Set up unit and keep it warm up at least 15 minutes.
c. Preset mode

IBM VGA	640X480	31.5KHz/60Hz
IBM VGA	640X400	31.5KHz/70Hz
SVGA4	800X600	46.88KHz/75Hz
6448B	640X480	43.27KHz/85Hz
SVGA3	800X600	48.09KHz/72Hz
SVGA5	800X600	53.6KHz/85Hz

3.1 B+ Adjustment : (For function test station only)

a. Input mode 53.6KHz (SVGA5) with cross hatch pattern.
b. Press "SELECT +" and "ADJUST -" keys at a same time.
c. Adjust switching power supply VR601 to make the horizontal B+ to be 43.5 +/- 0.2VDC.

3.2 Geometry Adjustment

a. Enter factory area -- Press "SELECT +" and "ADJUST-" at the same time then turn power switch on.
b. Press "ADJUST +" and "ADJUST -" at the same time to clear user area.
c. Input mode 31.5KHz (VGA 640x480) with tilt adjustment pattern.
d. Adjust CRT screw to meet tilt and orthogonal spec.
(Tilt < ±1 mm , Orthogonal < ±1.5mm)
e. Input the presetting modes and supporting modes with full white pattern.
f. Set external contrast to maximum and brightness to raster just cut-off position.
g. Press "SELECT +" or "SELECT -" to select the adjustment for H-size, H-phase, V-size, V-center, Pincushion or Trapezoid.
h. Press "ADJUST +" or "ADJUST -" to make the geometry can meet item 9 table 2 spec.
i. Press "SELECT +" and "ADJUST -" at the same time to save the adjustment data.
j. Change timing to next mode and repeat step f, g and h.
k. After all modes are adjusted OK, turn power switch off.

3.3 Background Adjustment

a. Enter factory area -- Press "SELECT +" and "ADJUST -" at the same time then turn power switch on.
b. Input mode 53.6KHz (SVGA5) with raster only pattern.
c. Adjust external brightness key to maximum.
d. Check the bias VRs of VR101, 102, 103 at counterclockwise maximum position.
e. Adjust screen VR of FBT to obtain twilight raster about 0.7 to 1.2 Ft-L.
f. See which gun appears first, then adjust the two bias VRs of the other two non-appearing guns to achieve the color temperature meet specification x=0.281 +/- 0.005
y=0.311 +/- 0.005
g. Adjust screen VR of FBT again to let the raster about 0.7 to 1.2 Ft-L.

3.4 Foreground Adjustment

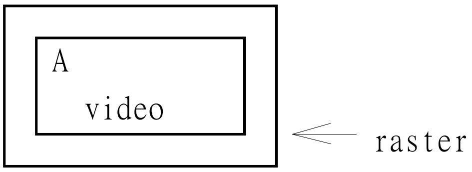
a. Input mode 53.6KHz (SVGA5) with 3-inch block pattern.
b. Check the drive VRs of VR104, 105 at center position.
c. Adjust external brightness key to cut-off and external contrast key to let the light output be 15 Ft-L.
d. Adjust VR103, 104 to let the color temperature meet the specification x=0.281 +/- 0.003
y=0.311 +/- 0.003
e. Adjust external contrast key to let light output be 45±3 Ft-L.
f. Press "SELECT +" and "ADJUST -" to save the adjustment data.
g. Adjust VR301 to let light output be 30±0.5 Ft-L.
h. Turn power switch off.

3.5 Final Check

a. Enter final check area -- press "SELECT +" and "ADJUST +" at the same time then turn power switch on.
b. Input mode 53.6KHz (SVGA5) with full white pattern.
c. Press "SELECT +" and "ADJUST -" keys at a same time.
d. Check the light output is greater than 30Ft.L.
e. Adjust external contrast and brightness keys to minimum, the video and raster should be disappear.
f. Check the performance of all modes can meet spec.

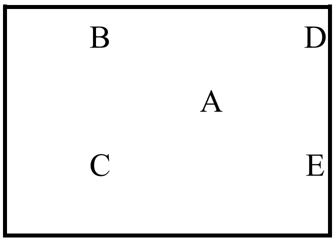
3.6 Focus Adjustment

a. Input mode 53.6KHz (SVGA5) with characters pattern.
b. Press "SELECT +" and "ADJUST -" keys at a same time.
c. Adjust focus VR of FBT to make "A" area focus clear.



3.7 Convergence Adjustment

a. Input mode 53.6KHz (SVGA5) with purple cross hatch pattern.
b. Adjust 4-pole magnetic ring of Yoke to meet specification.
c. Input mode 53.6KHz (SVGA5) with yellow cross hatch pattern.
d. Adjust 6-pole magnetic ring of Yoke to meet specification.
e. Input mode 53.6KHz (SVGA5) with white cross hatch pattern.
f. Re-confirm the mis-convergence can meet spec.



A $\leqq$ 0.2 mm

B,C,D,E $\leqq$ 0.3 mm

3.8 Power Saving Function Check

a. Input mode 53.6KHz (SVGA5) with full white pattern.
b. Set external contrast and brightness keys to maximum position.
c. Remove H-Sync only, the video and raster should be extinguished. The LED shows green color and the power consumption should be less than 60W.
d. Remove V-Sync only, the video and raster should be extinguished.
The LED shows orange blink and the power consumption should be less than 5W.
e. Remove both H and V Sync, the power consumption should be less than 5W and LED shows orange blink.
f. Input H-Sync and V-Sync, the video should be exhibited again and LED on (green).

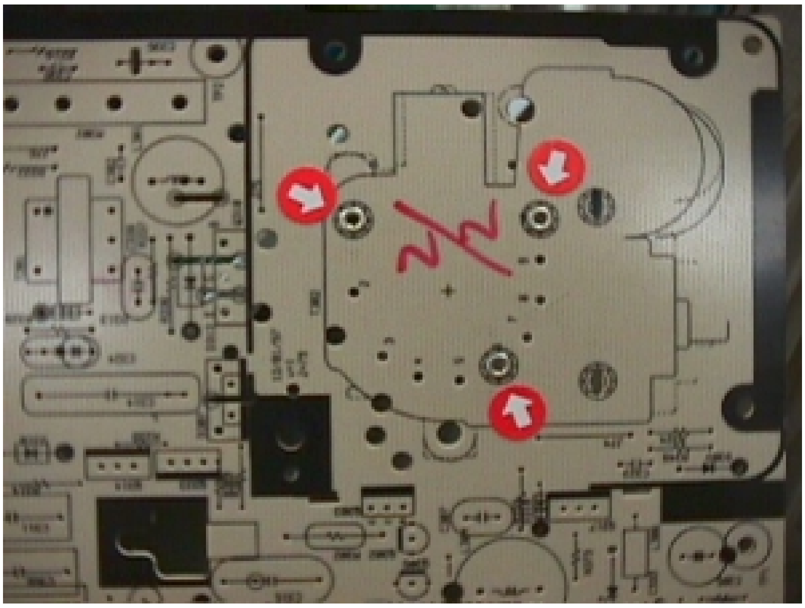
3.9 Geometry Specification for Production Line

(Table 2)

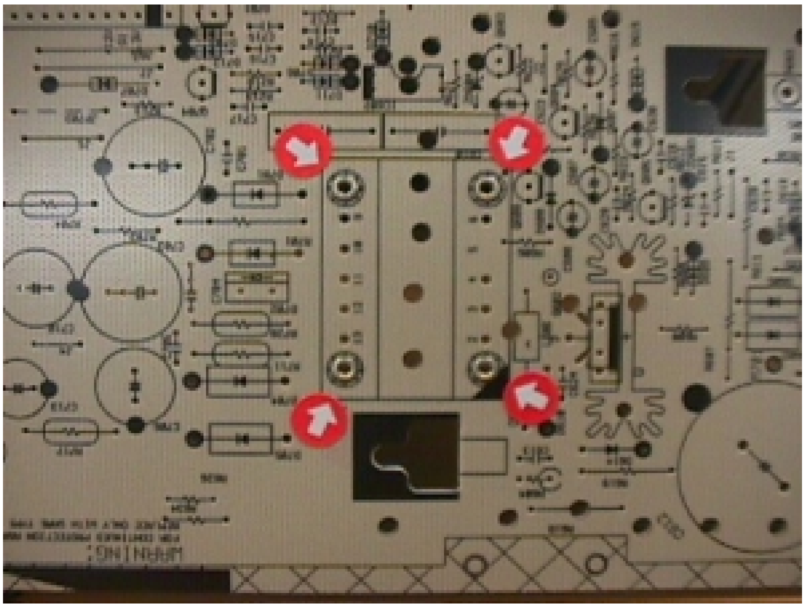
ITEM	DESCRIPTION	SPECIFICATION
1	HORI SIZE	270±4 mm
2	VERT SIZE	202±4 mm
3	SIDE PIN	≦ 2.0 mm
4	TOP/BOTTOM PIN	≦ 1.0 mm
5	SIDE BARREL	≦ 1.0 mm
6	TOP/BOTTOM BARREL	≦ 1.0 mm
7	TRAPEZOID	≦ 1.0 mm
8	VIDEO OFFSET	≦ 4.0 mm
9	PARALLELGRAM	≦ 2.0 mm
10	HORI LINEARITY	≦ 5 %
11	VERT LINEARITY	≦ 5 %

3.10 Eyelet parts:

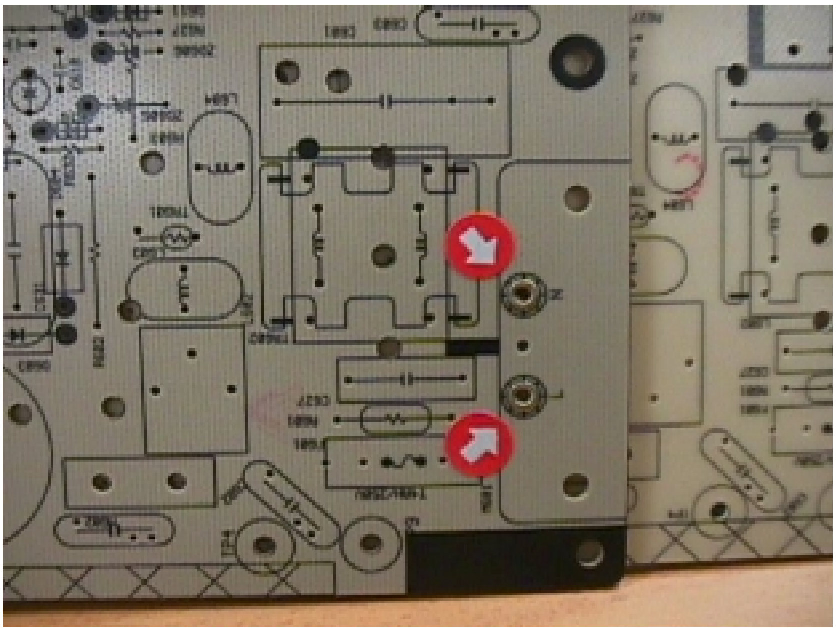
3.10.1 T302: 3 points



3.10.2 T601: 4 points



3.10.3 M601: 2 points

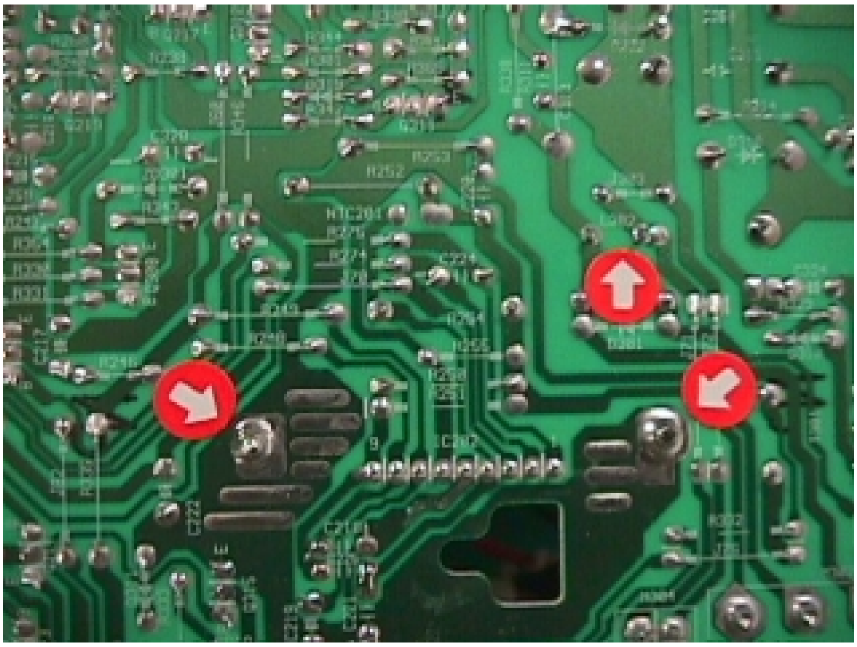


3.11 Touch-up parts:

The component listed below must touch-up to avoid solder crack.

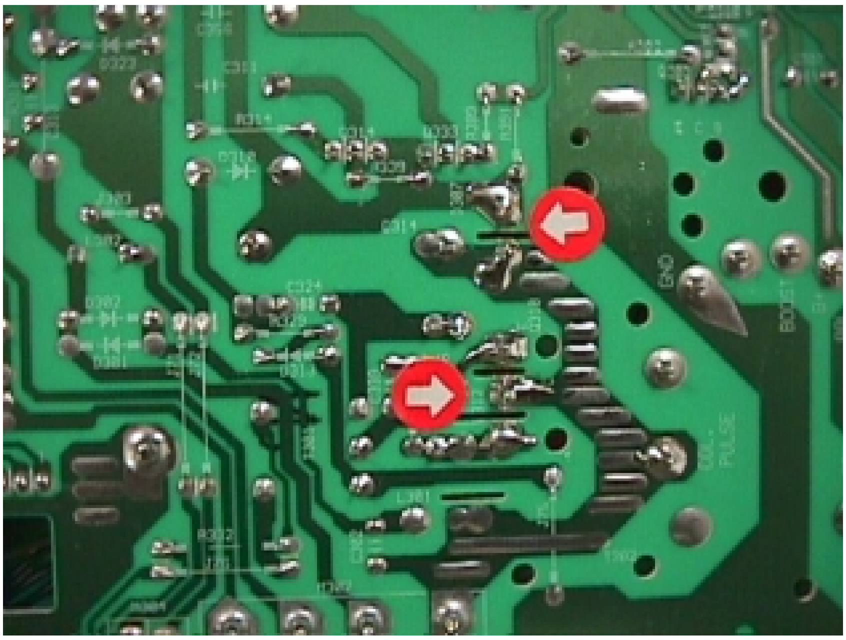
3.11.1 IC202: 2 points

3.11.2 L302: 2 points



3.11.3 Q310: 3 points

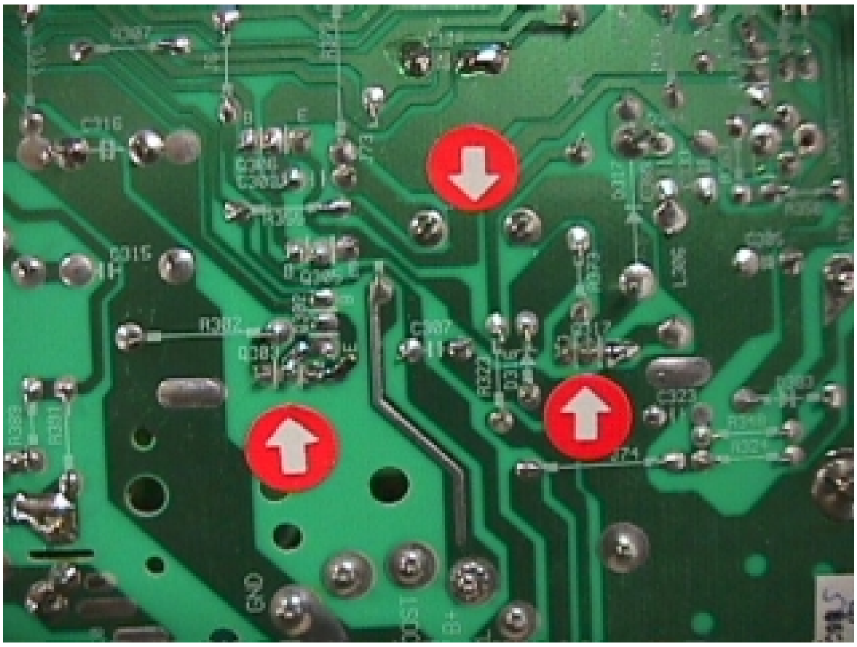
3.11.4 D307: 2 points



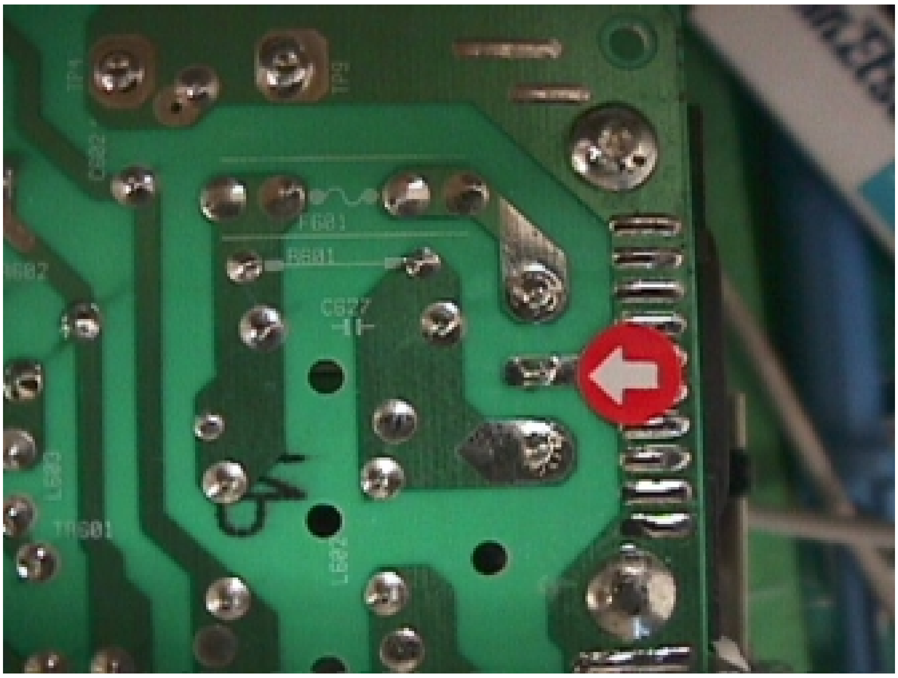
3.11.5 Q303: 3 points

3.11.6 Q317: 3 points

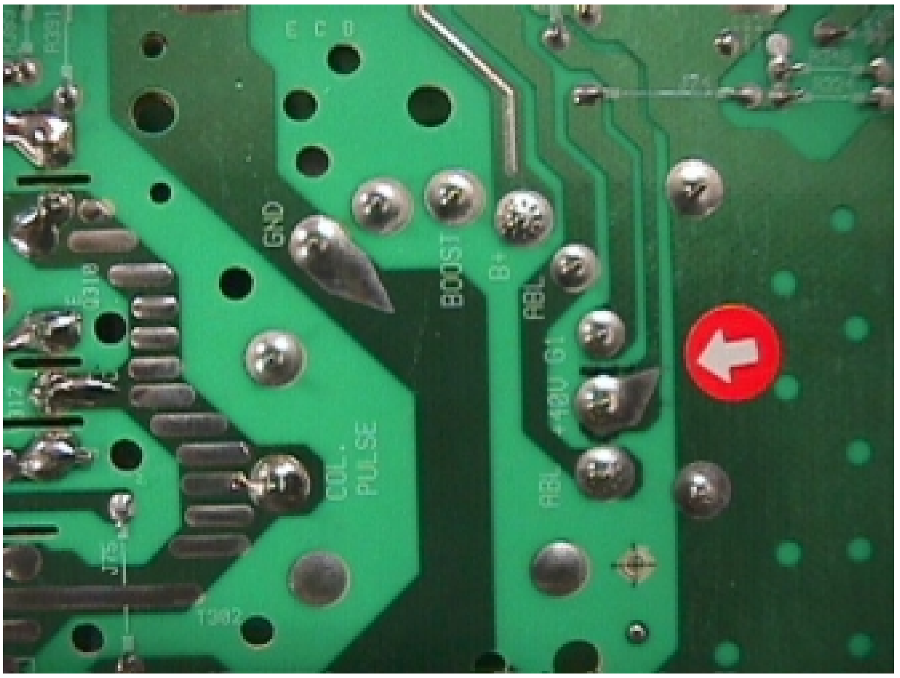
3.11.7 L304: 2 points



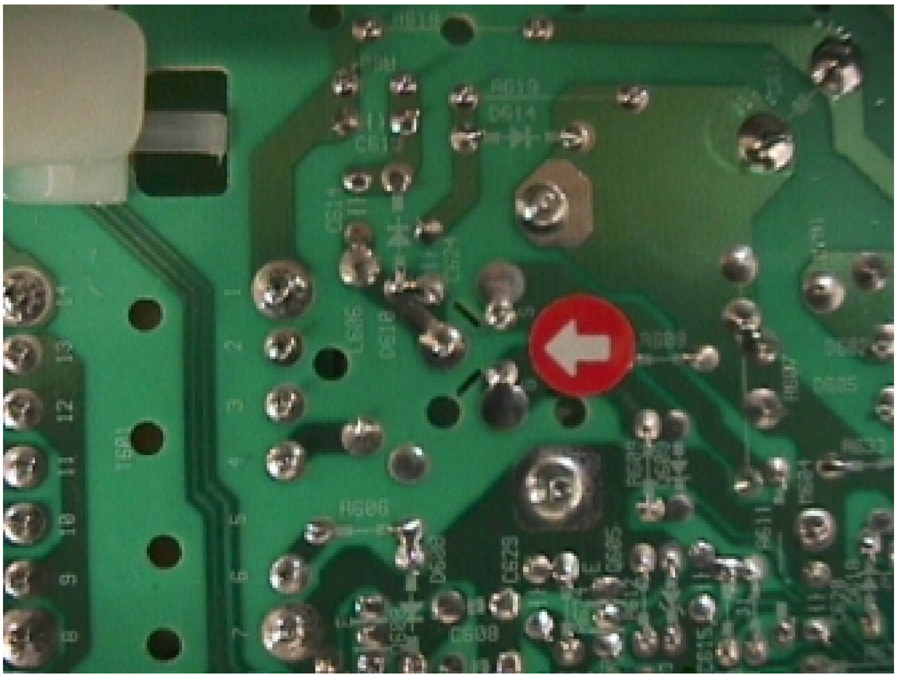
3.11.8 M601: 3 points



3.11.9 T302: 12 points



3.11.10 Q602: 3 points

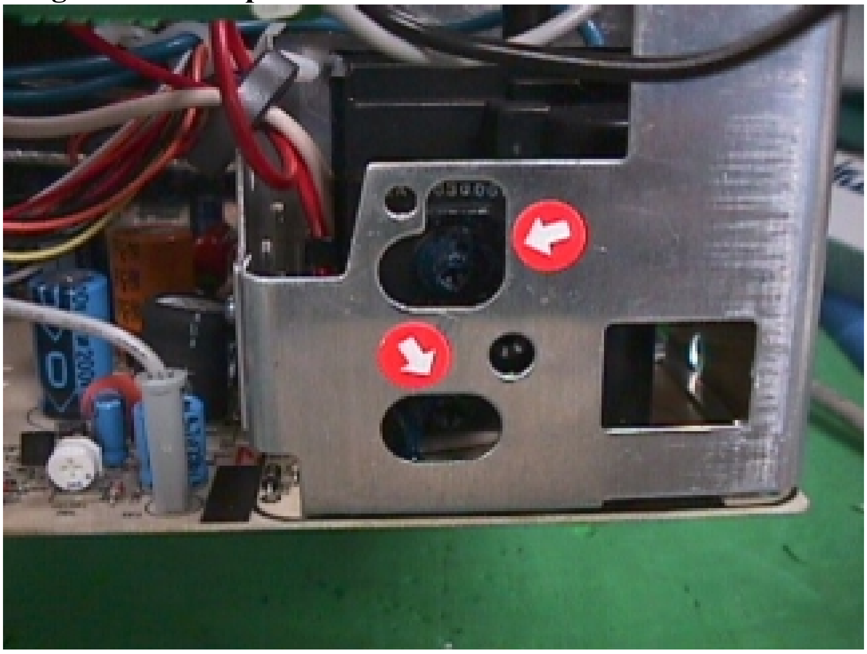


3.11.11 M101(CRT socket): 8 points

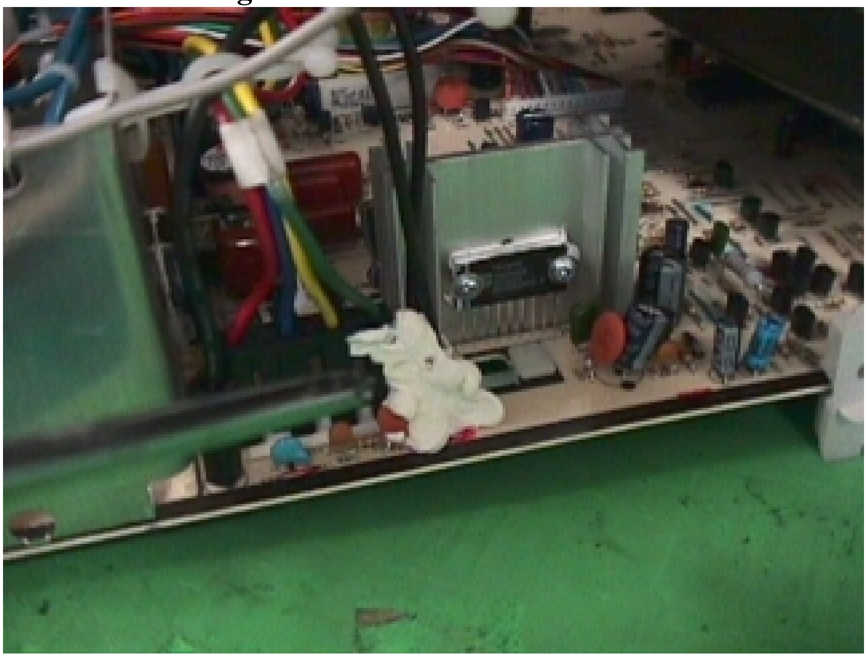


3.12 Glue parts:

3.12.1 G2 & G4 VR add glue to fix the position of VR



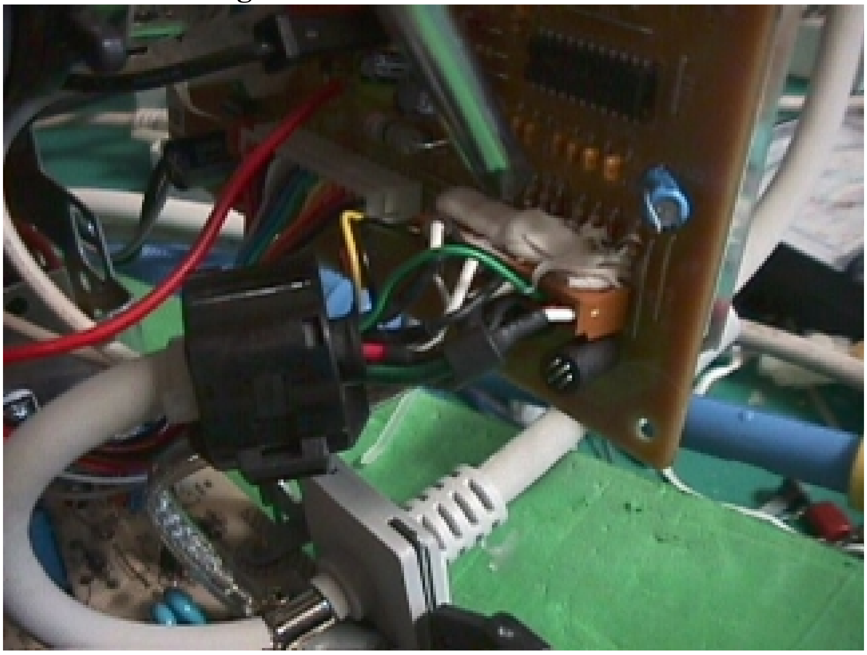
3.12.2 M304 add glue to fix the housing



3.12.3 L603 & L604 add glue to fix the housing

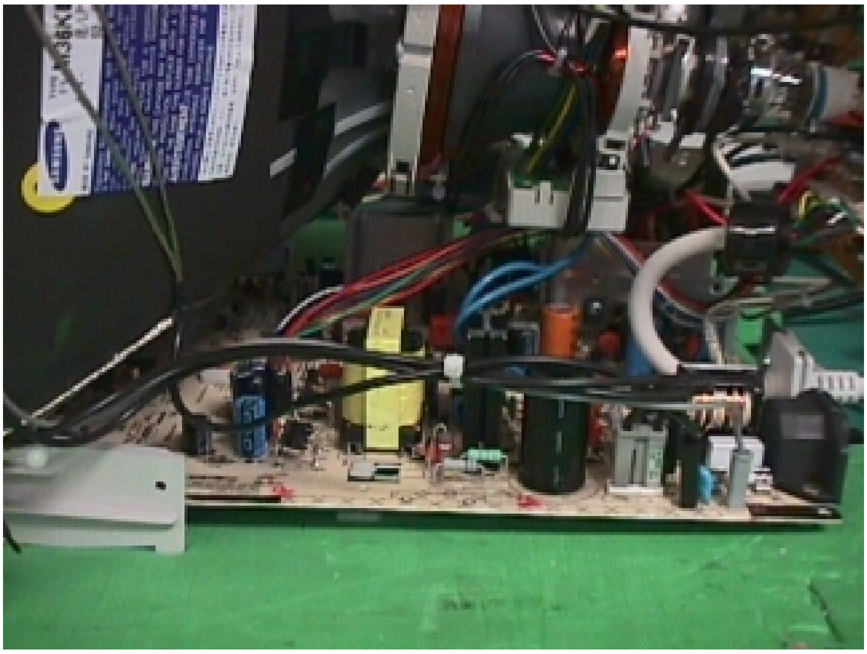


3.12.4 M102 add glue to fix the housing

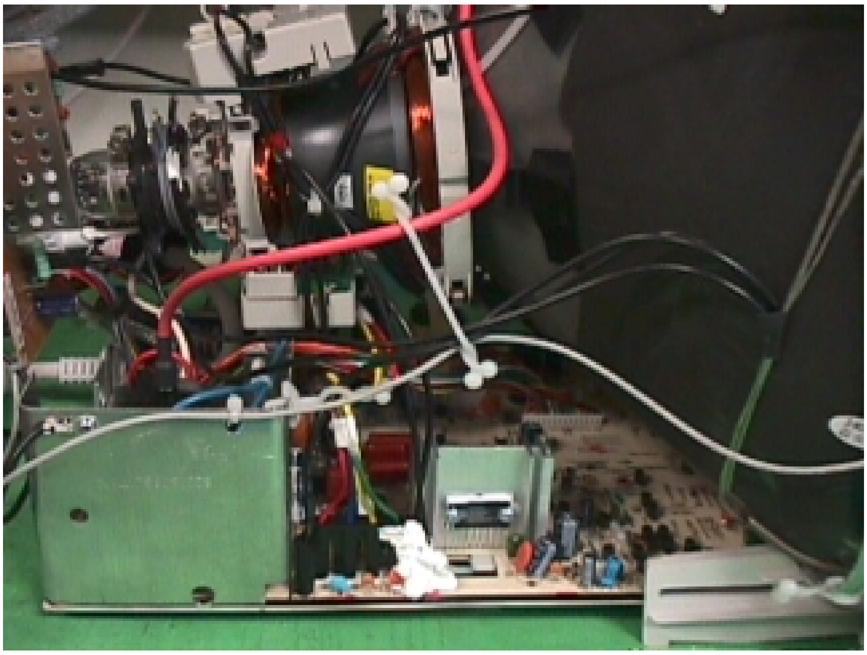


3.13 Wire Dressing parts:

3.13.1 Left side view:



3.13.2 Right side view:



3.13.3 Rear side view:

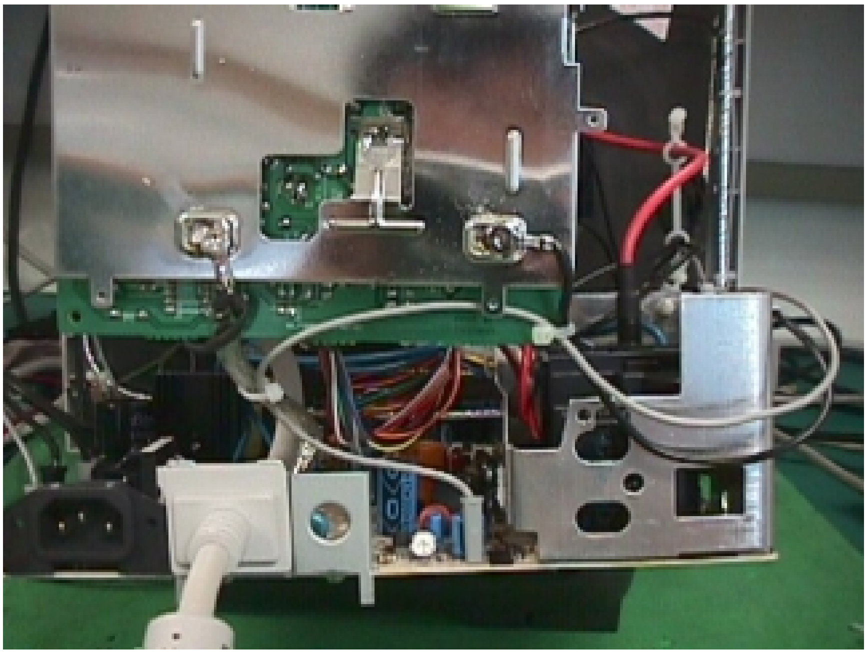
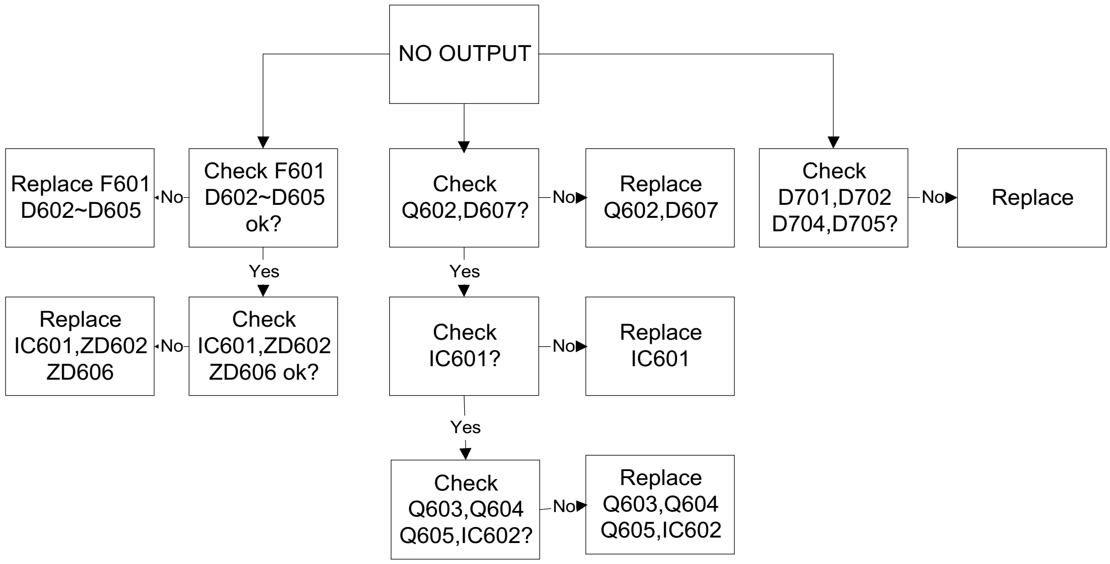
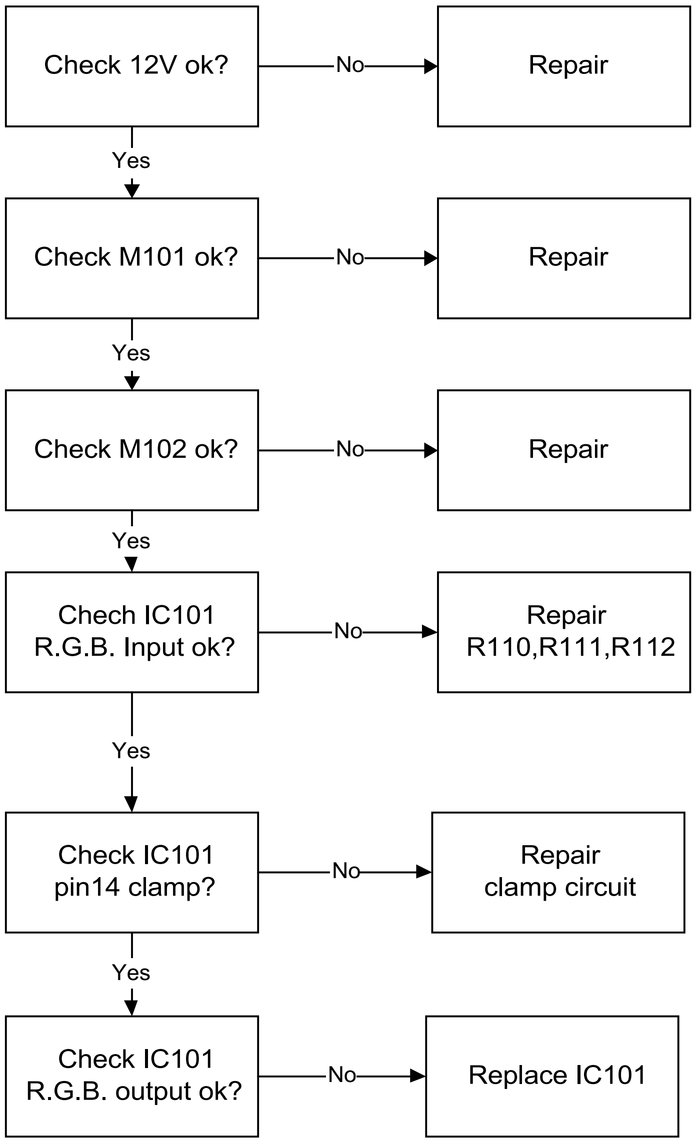


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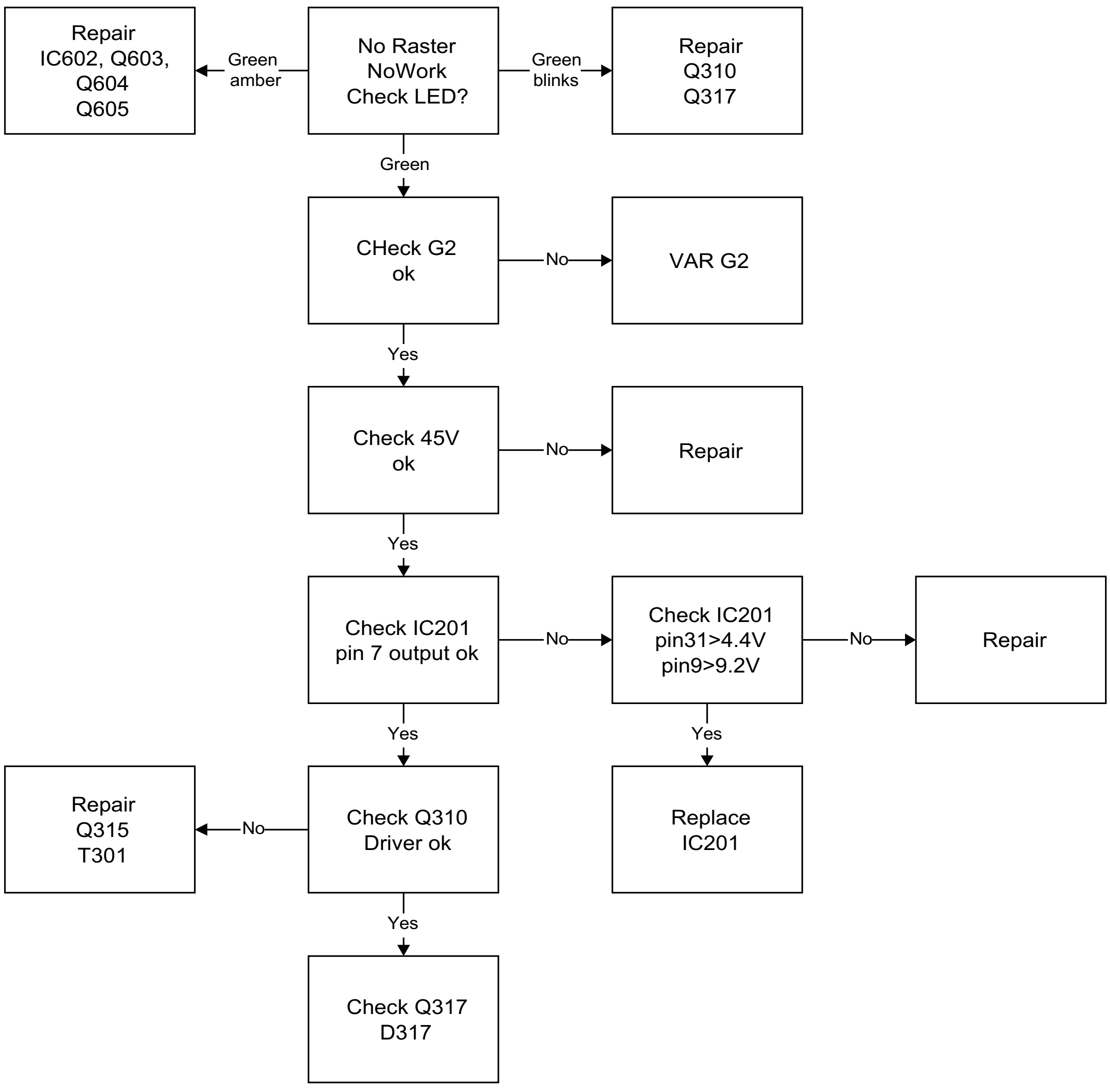
4.1 No Output Power



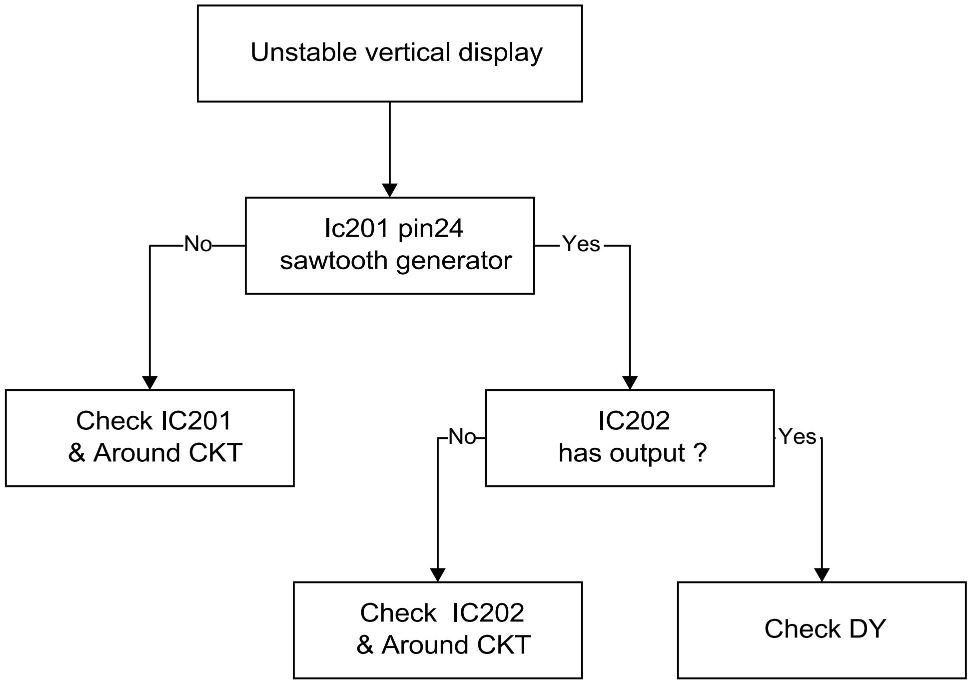
4.2 No Video


Check 12V ok?
No
Repair
Yes
Check M101 ok?
No
Repair
Yes
Check M102 ok?
No
Repair
Yes
Chech IC101
R.G.B. Input ok?
No
Repair
R110,R111,R112
Yes
Check IC101
pin14 clamp?
No
Repair
clamp circuit
Yes
Check IC101
R.G.B. output ok?
No
Replace IC101

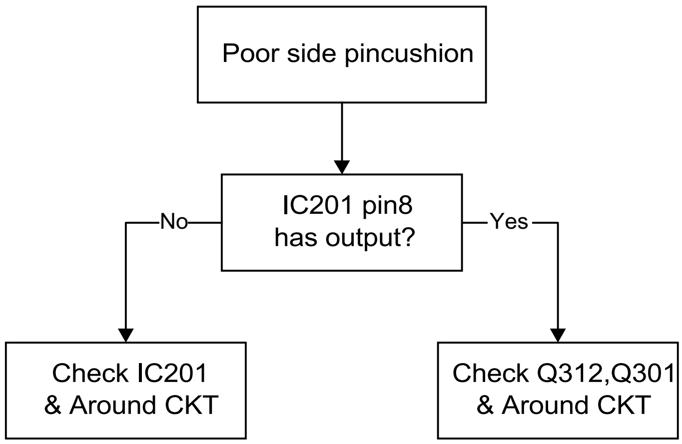
4.3 No Raster / No Work



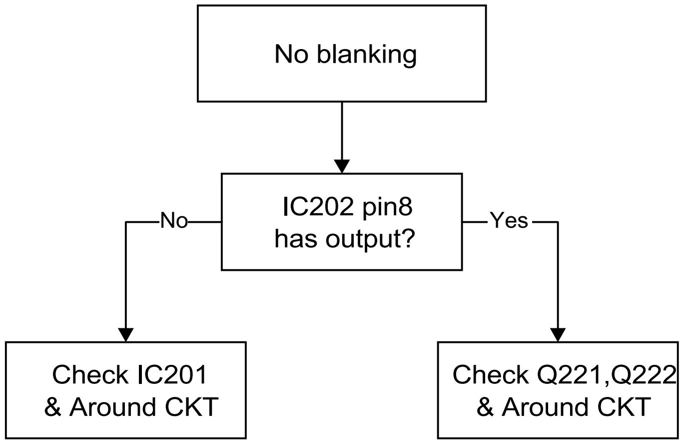
4.4 Unstable Vertical Display



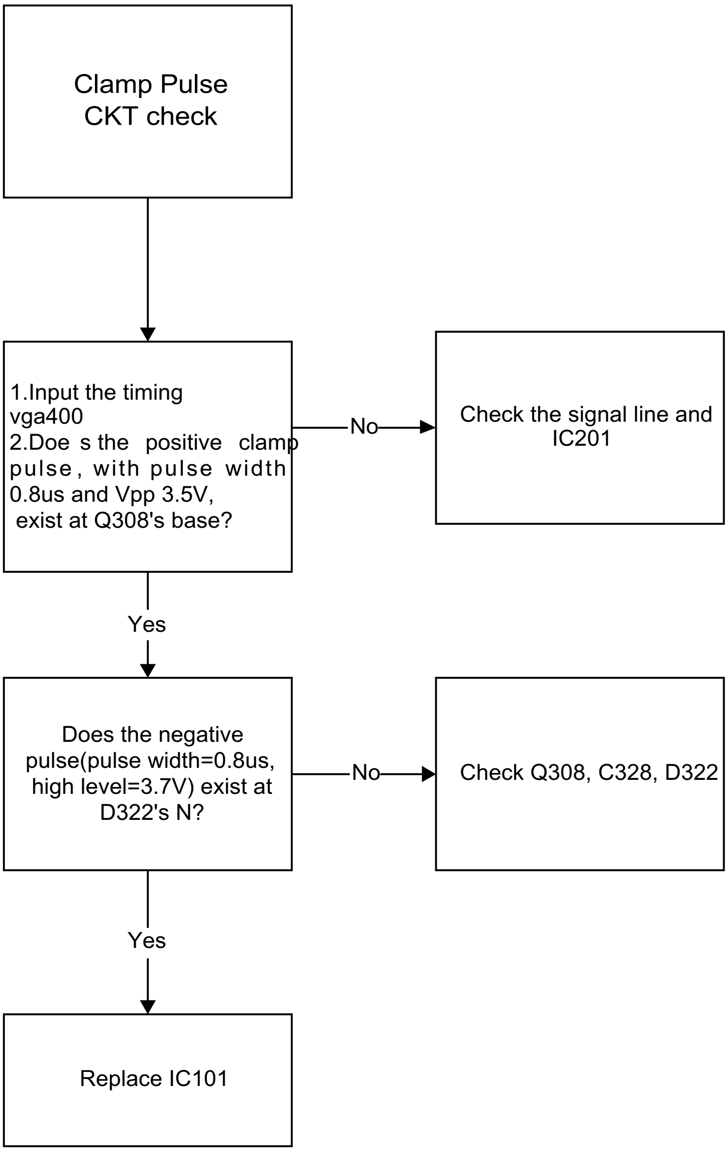
4.5 Poor Side Pincushion



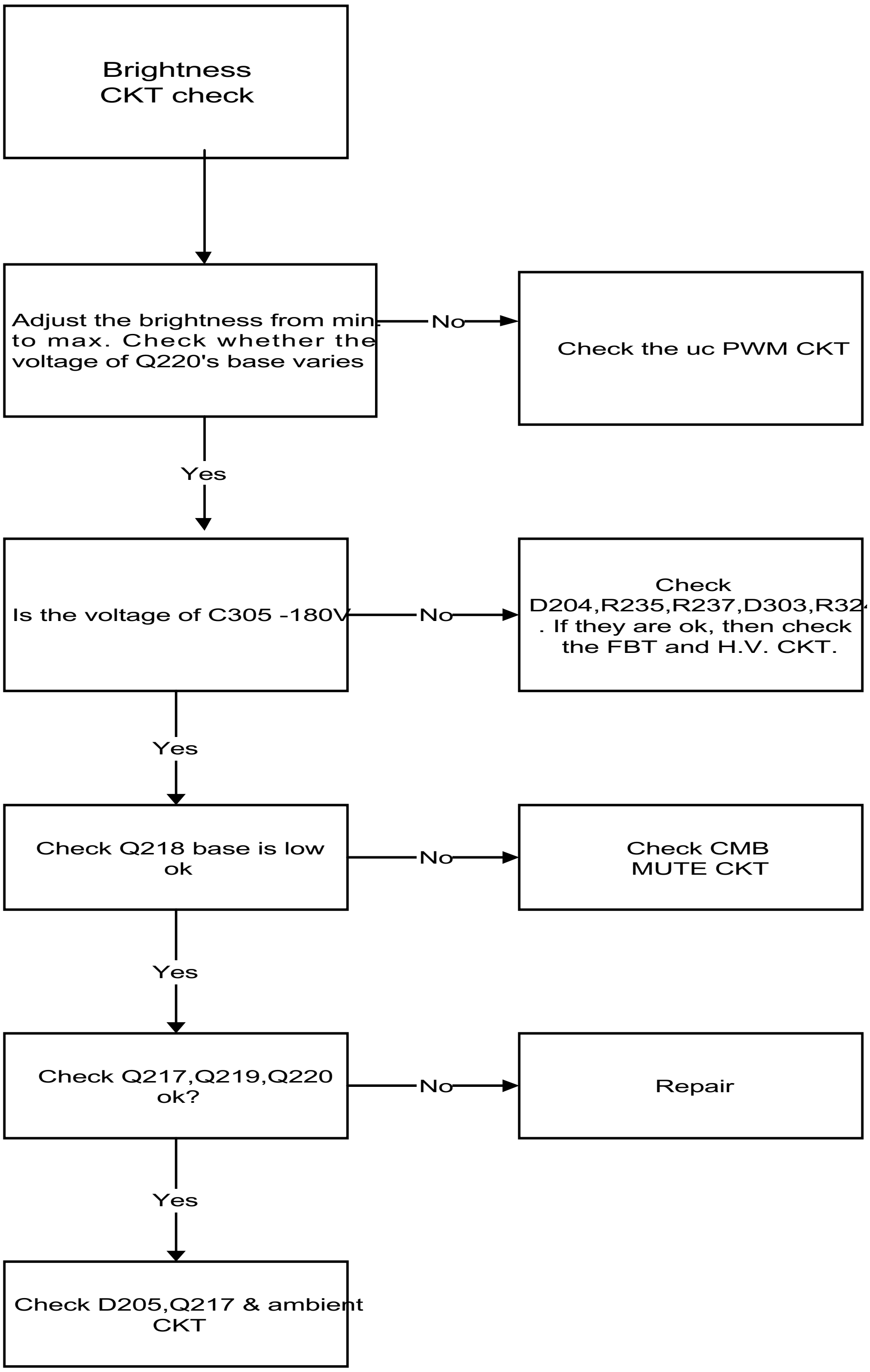
4.6 No Blanking



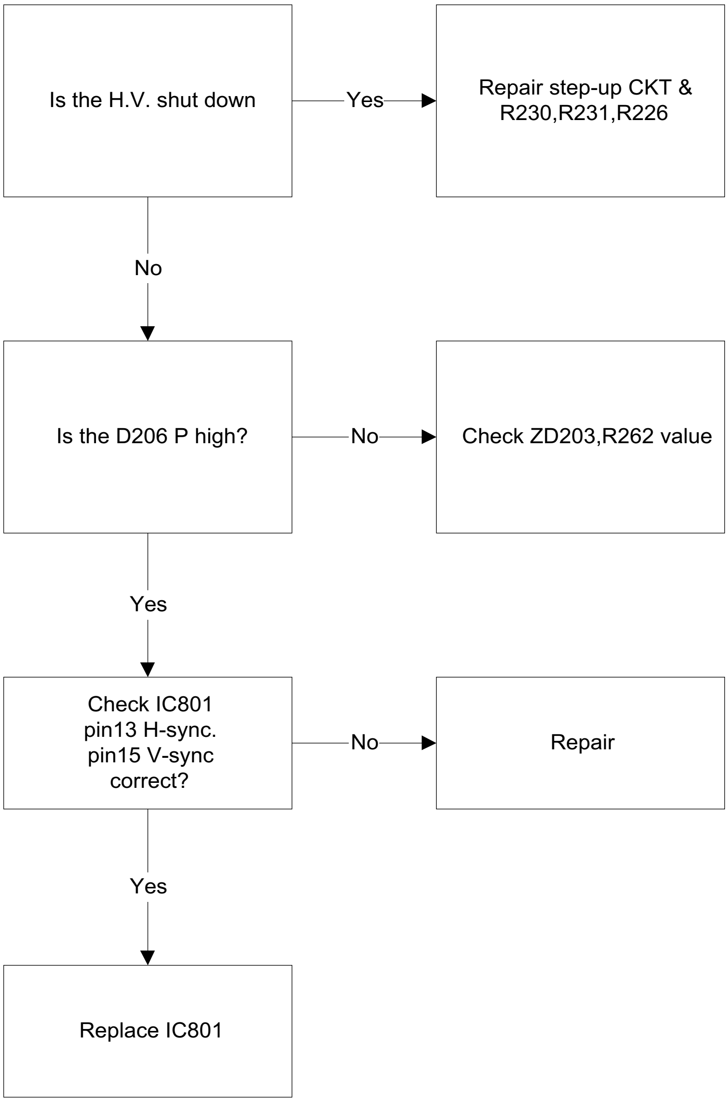
4.7 Clamp Pulse CKT Check



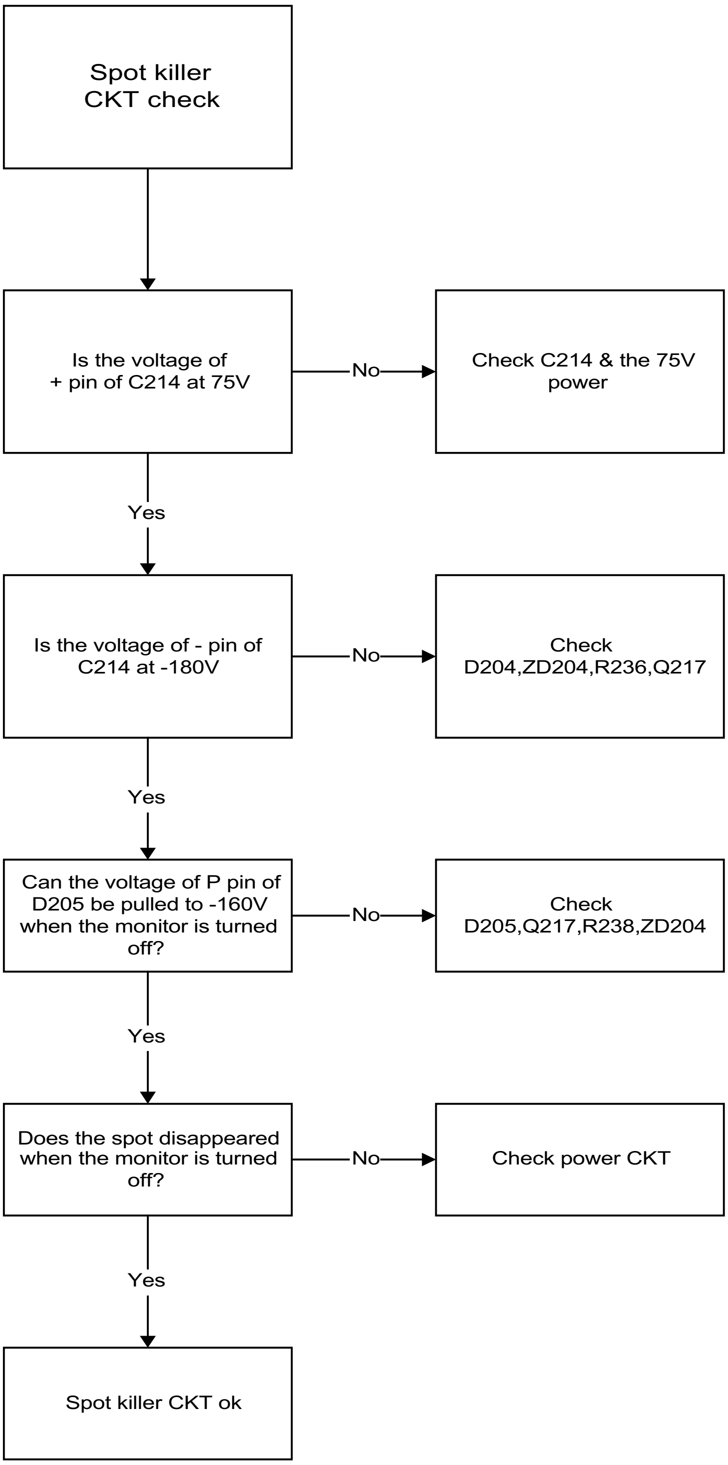
4.8 Brightness CKT Check

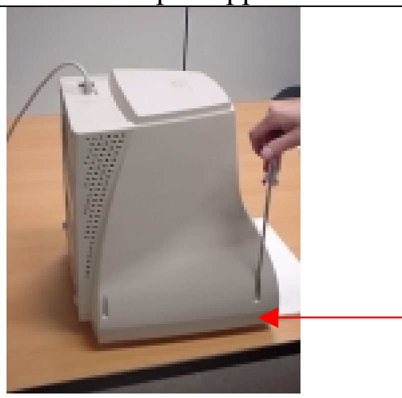
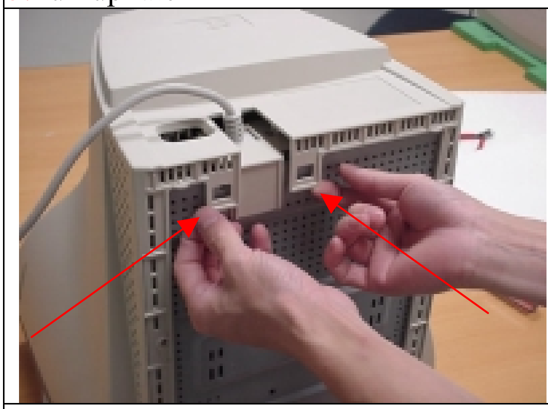
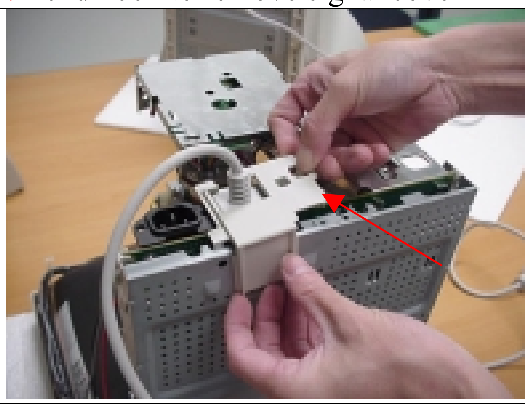
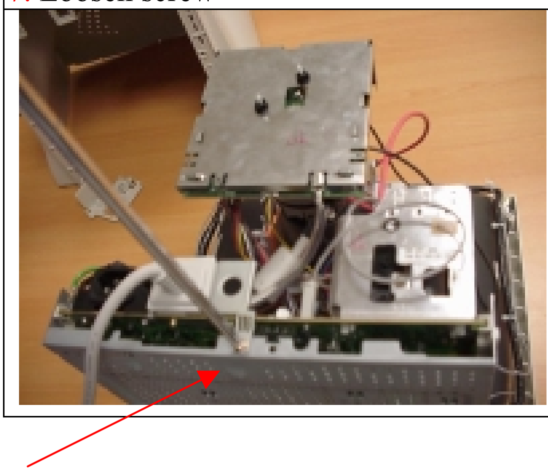
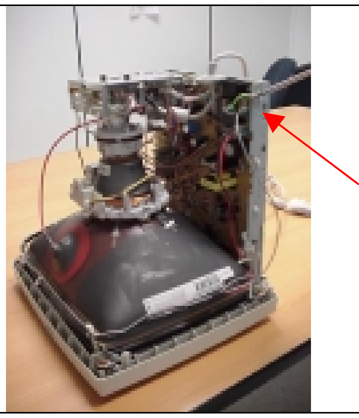


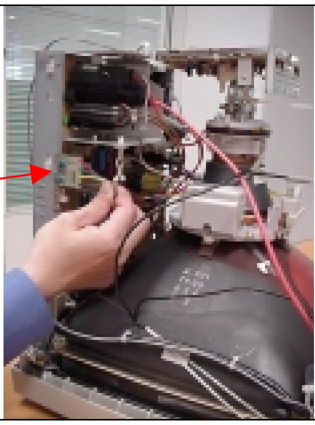
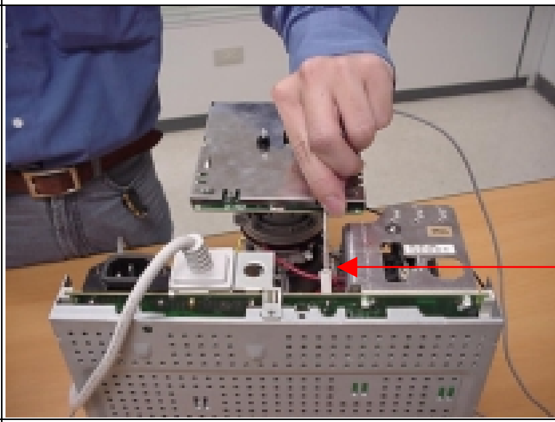
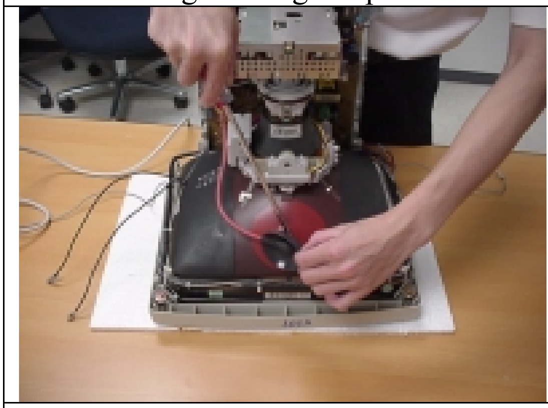
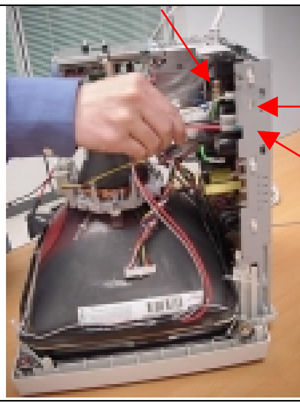
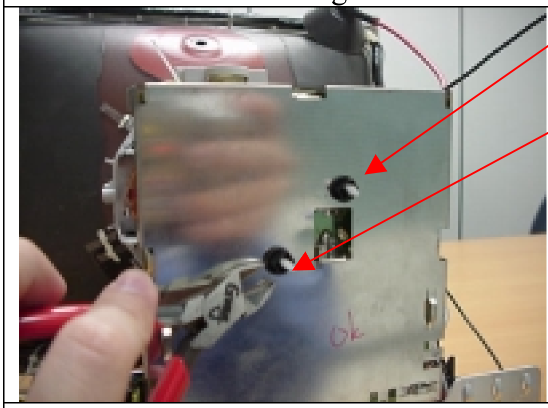
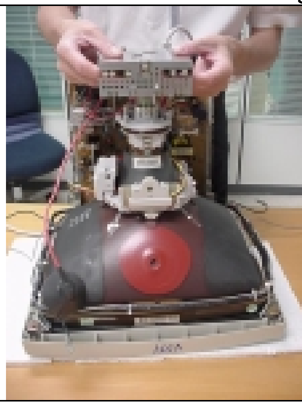
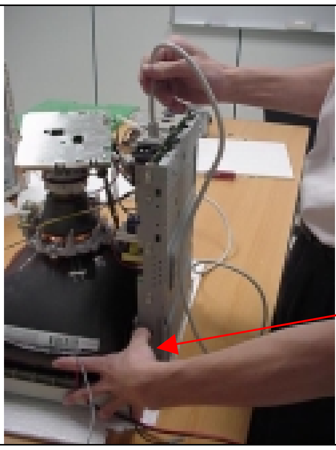
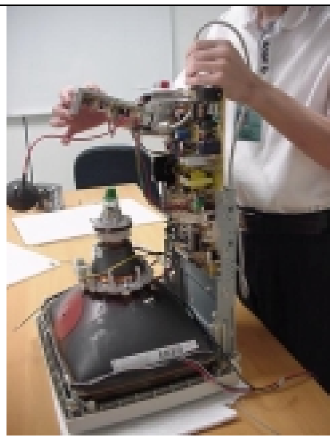
4.9 Change Mode Blanking (C.M.B.) and Mute CKT



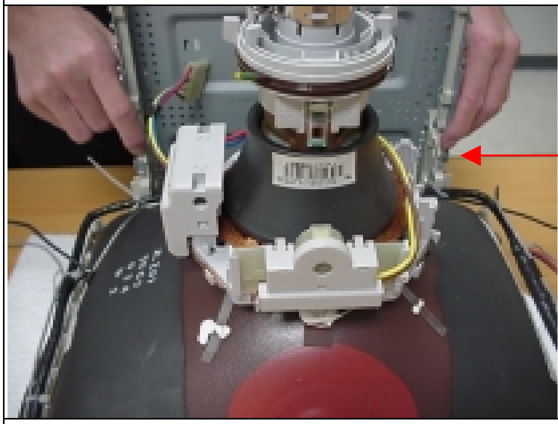
4.10 Spot Killer CKT Check



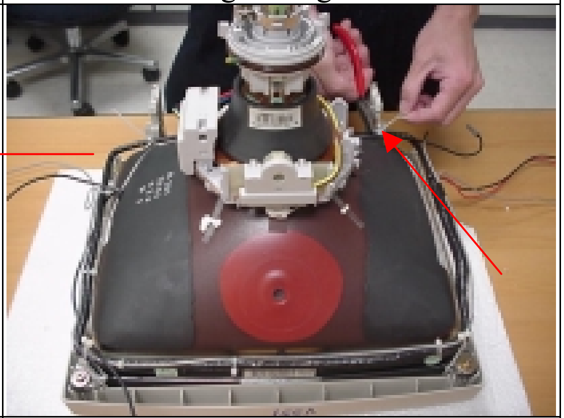
1.Front view of Monitor:	2.Side view of Monitor
	
3.Back view of Monitor	4.Loosen screw and open upper case
	
5.Pull up latch	6. Bend hook to remove signal cover
	
7. Loosen screw	8.Loosen screw
	

9. Remove connectors	10. Remove connectors
	
11. Loosen High Voltage Cap	12. Remove connectors
	
13. Cut off tie of shielding board	14. Pull out video board shielding
	
15. Bend hook to remove main board	16. Pull out Main Board
	

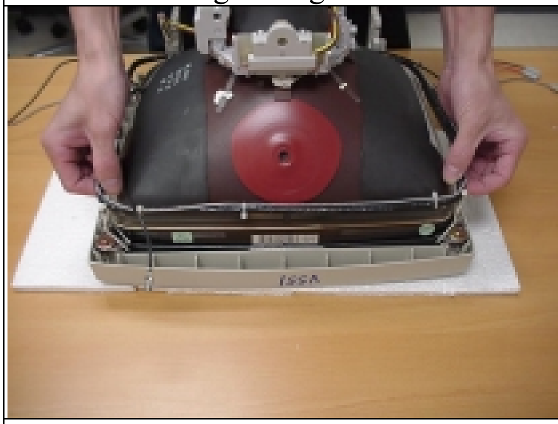
17. Press down hook to remove bracket



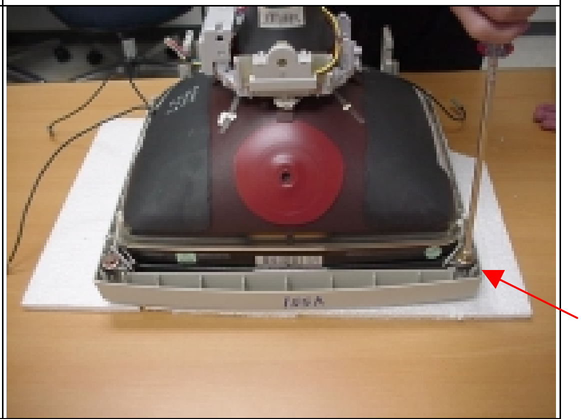
18. Cut tie of Degaussing Coil



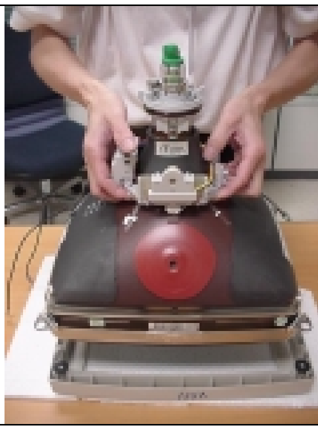
19. Take out Degaussing Coil



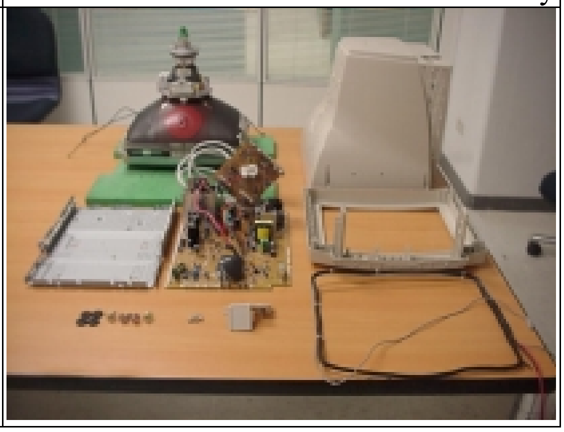
20. Loosen CRT's screw



21. Take out CRT



22. Overview of monitor after disassembly



P/N: 91.71602.057

Item	P/N	Description	Location
1	55.71601.721	MAIN BD V551/7254E-MI	
2	55.71602.081	VIDEO BD V551/7254E-MI	
3	39.90803.001	UC W/O SPK/CORE ABS 002 V551	
4	60.71655.001	ASSY BZL ABS94V0 002 54E/V551	
5	60.90801.011	ASSY BASE HI-PS 002 V551/ALL	
6	60.90803.001	ASSY SIGNAL/C 7254E/V551/ACER	
7	56.05785.191	CRT 15"M36EDR 320X304/2F01	
8	19.90029.021	COIL DEGAUSSING 7154E/LR FRONT	
9	42.77504.031	PE BAG LDPE 750*790 ALL	
10	44.90801.001	CTN AB 458*424*392 V551/ACER	
11	47.90801.001	CUSHION-TOP EPS V551/ACER	
12	47.90802.001	CUSHION-BTM EPS V551/ACER	
13	27.82718.011	CORD H05VV-F#18*3C 10A 250V EUR	
14	49.71601.331	MANUAL USER ACER V551 MPRII 6L	
15	01.03524.002	IC UCTRL AP3524-2 DIP 40P	IC801
16	02.02404.000	IC EEPROM 24C04 4K-BIT DIP 8P	IC804 **
17	04.03842.044	IC VR UC3842BN DIP 8P	IC601
18	04.04858.070	IC SYNC CTRL TDA4858 DIP32	IC201
19	05.00721.010	PHOTO TLP721F DIP 4P	IC602
20	06.00630.020	FET MOS IRF630 NV TO-220	Q333 Q314
21	06.2R010.120	DIODE FAST RGP20BL-5300 100V2	D705
22	06.2R020.121	DIODE FAST EGP20D 200V 2A	D704
23	06.2R320.120	DIODE F BYM26A 2.3A200V SOD64	D317
24	06.3R060.123	DIODE FAST BYM36C 600V 3A	D702 D308
25	08.33217.303	CAP DISC Y 3300P U/V/FI R	C602 C603
26	09.15717.014	CA[E; 150U 400V M RF10	C612
27	11.10437.03E	CAPACITOR MPE 0.1U 400V J RF15	C631
28	11.2241N.11K	CAP X 0.22U U/V/FI 275V RF22.5	C601
29	11.30437.06K	CAP MPP 0.3U J 400V RF22.5	C312
30	11.3923B.05K	CAP PPS 3900P 1.6KV J RF22.5	C314
31	11.56238.05E	CAPACITOR PP 5600P 630V J RF15	C315
32	13.33335.03H	RES MOF 33K J 2W AF20	R602 R603
33	13.39335.074	RES MOF 39K J 2W RF5 MINI	R604
34	13.47135.07E	RES MOFM 470 J 2W AF15 MINI	R619

P/N:91.71602.057

Item	P/N	Description	Location
35	13.R2235.07E	RES MOFM 0.22 J 2W AF15 MINI	R607
36	17.40010.202	SVR 2K B 6D 5*5 H	VR601
37	17.40016.203	SVR 20K B 6D 5*2.5V	VR301
38	17.60017.00A	THERM 100/14 PTC 18*13*18	TR602
39	17.60021.8R0	THERM 8 NTC 11.5D	TR601
40	19.20079.011	XFORM EI-19 56E/T302	T302
41	19.20079.091	XFORM PWR ERL35 250UH 34E/T601	T601
42	19.40054.011	CHOK 180UH T50-26 7033	L603 L604
43	19.40087.001	LINE FILTER 18MHZ EE28 7134T	L602
44	19.40108.011	CHOKE 150UH DRWW14*15 54E/L303	L303
45	19.40139.001	CHOKE 1.5MH DR16*18 7234E/L304	L304
46	19.70060.001	FBT TRANSFORMER E551 7254E	T302
47	23.30008.721	XTAL 12MHZ 30P 20PPM RF5	Y801
48	26.14001.113	FUSE 4A 250V ST20 L/H SEM/U	F601
49	04.78L05.030	IC V.R 78L05 P TO-092 3P(TI)	IC802
50	06.00422.010	XTOR BF422 TO-92T NPN P RT	Q217
51	06.00423.010	XTOR BF423 TO-92T PNP P RT	Q219
52	06.00844.01A	TRANSISTOR 2SA844 C TO-92T PNP	Q701 Q704
53	06.02235.010	XTOR 2SC2235 Y TO-92T NPN P RT	Q315
54	06.18R03.070	DIODE ZEN 18V 1/2W DO-35 5%	ZD602
55	06.1R002.110	DIODE S.B. 1N5817 20V 1A DO-41	D312
56	06.1R005.030	DIODE REC 1N4001 50V 1A DO-41	D607
57	06.1R010.030	DIODE REC 1N4002 100V 1A DO-41	D304
58	06.1R020.030	DIODE REC 1N4003 200V 1A DO-41	D323 D204 D205 D104
59	06.1R020.121	DIODE FAST RGP10D 200V 1A	D608
60	06.1R040.030	DIODE REC 1N4004 400V 1A DO-41	D303
61	06.1R060.030	DIODE REC 1N4005 600V 1A DO-41	D356 D305
62	06.1R060.120	DIODE FAST RGP10J 600V 1A	D610 D614 D310
63	06.1R0A0.122	DIODE FAST UF4007 1KV 1A	D701
64	06.24R03.070	DIODE ZEN 24V 1W DO-41 + -5%	ZD605
65	06.2R060.030	DIODE REC 20D6 600V 2A DO-41	D602-605
66	06.2R403.070	DIODE ZEN 2.4V 1/2W DO-35 5%	ZD301
67	06.30R03.071	DIODE ZEN 30V 1/2W DO-35 5%	ZD203 ZD206 ZD606
68	06.3R303.070	DIODE ZEN 3.3V 1/2W DO-35 5%	ZD604

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Item	P/N	Description	Location
69	06.5R103.070	DIODE ZEN 5.1V 1/2W DO-35 5%	ZD603 ZD201 ZD202 ZD204 ZD801-804
70	06.5R603.070	DIODE ZEN 5.6V 1/2W DO-35 5%	ZD805
71	06.9R103.070	DIODE ZEN 9.1V 1/2W DO-35 5%	ZD205
72	08.1021A.03W	CAP DISC 1000P 1KV M Z5U RT5	C705
73	08.1031G.03W	CAP DISC 0.01U 500V Z5U RT5	C308 C309
74	08.2212G.13W	CAP DISC 220P 500V K Y5P RT5	C317
75	08.3321A.03W	CAP DISC 3300P 1KV M Z5U RT5	C613
76	08.5612A.13W	CAP DISC 560P 1KV K Y5P RT5	C624 C336
77	09.47416.01W	CAP EL 0.47U 250V M RT5	C217
78	09.47516.01W	CAPACITOR EL 4.7U 250V M RT5	C305
79	09.4751K.01W	CAP EL 4.7U 350V M RT5	C214
80	13.30133.012	RES 300J 1/2W	R311
81	06.00630.021	FET MOS YTAF630 NC SC-67	Q317
82	06.00669.01A	XTOR 2SD669A C TO-126 NPN P	Q303
83	06.02508.010	XTOR BU2508AF SOT199 NPN P	Q310
84	06.5R0F0.030	DIODE REC FMP-G2FS 1.5KV 5A	D307
85	06.00060.021	FET MOS SSS6N60A NC TO-220	Q602
86	04.01375.010	IC VIDEO AMP MM1375XD DIP 22P	IC101
87	06.01609.010	XTOR 2SD1609 C TO-126 NPN P	Q101 Q103 Q105
88	13.12236.07H	RES MOF 1.2K J 3W AF20 MINI	R151-153
89	06.1SS83.040	DIODE SW 1SS83 300V 0.2A DO-35	D101-103
90	08.1021C.03W	CAP DISC 1000P 2KV M Z5U RT5	C127
**	Please provide CRT, Customer, Model, Location and EEProm Type when you order EEProm IC. Then, we could write program in advance		
!	The components identified by the mark of ! in the schematic are important X-Radiation and Safety Parts. Should replacement is required, replace only with the same type and rating originally used.		
*	The components identified by the mark of * in the schematic are import safety parts. If replacement is required, refer to service manual to re-adjust or re-checked the B+ and High Voltage.		